Access DB# 64153

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: Lynette T. Umez-Eronini Examiner #: 74987 Date: 4/9/2002
Art Unit: 1765 Phone Number 30 6-9074 Serial Number: 09/945508
Mail Box and Bldg/Room Location: 10E17 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: Nitride selective and field oxide selective semiconductor etching
Inventors (please provide full names): Kei-yu [redacted] Ko

Earliest Priority Filing Date: 8/30/2000

For Sequence Searches Only *Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

Search claims 1, 6, and 12

where "a carrie gas" is Ar, He, and Xe;

where $C_{2+}F$ is C_3F_6, C_3F_8, C_4F_6, C_4H_8 and C_5H_8

Also search etching or etchant
"silicon nitride" or semiconductor
or "silicon oxide"

****

STAFF USE ONLY

Searcher: John Calve
Searcher Phone #: 308-4139
Searcher Location: _____
Date Searcher Picked Up: 4/10/02
Date Completed: 4/10/02
Searcher Prep & Review Time: 2 hr
Clerical Prep Time: _____
Online Time: 2 hr

Type of Search

NA Sequence (#) _____
AA Sequence (#) _____
Structure (#) _____
Bibliographic ✓
Litigation _____
Fulltext _____
Patent Family _____
Other _____

Vendors and cost where applicable

STN ✓ $479.51
Dialog _____
Questel/Orbit _____
Dr.Link _____
Lexis/Nexis _____
Sequence Systems _____
WWW/Internet _____
Other (specify) EAST - Dennett.

PTO-1590 (8-01)

=> d his full

FILE 'HCAPLUS' ENTERED AT 14:16:38 ON 10 APR 2002
L1 10 SEA KO KEI-YU/IN

FILE 'REGISTRY' ENTERED AT 14:24:47 ON 10 APR 2002
E C3H2F6/MF
L2 7 SEA C3H2F6/MF

E 3F8/MF
E C3F8/MF
L3 3 SEA C3F8/MF
L4 23 SEA C4H4F6/MF
E C4H2F8/MF
L5 12 SEA C4H2F8/MF
E C5H4F8/MF
L6 33 SEA C5H4F8/MF
E C4H2F8/MF
L7 12 SEA C4H2F8/MF
E CHF3/MF
L8 8 SEA CHF3/MF
E CF4
L9 139 SEA CF4/~~DI~~ MF
L10 106 SEA (C(L)F)ELS (L) 2/ELC.SUB CF

C(L)H(L)(F)

E HEXAFLUOROPROPANE/CN
E OCTAFLUOROPROPANE/CN
E PERFLUOROPROPANE/CN
L11 1 SEA ARGON/CN
E HELIUM/CN
L12 1 SEA HELIUM/CN
E XENON/CN
L13 1 SEA XENON/CN

Si N
Silicon nitride
Si O

L14 2159157 SEA GAS## OR GASEOUS? OR GASIF? OR VAPOR? OR VAPOUR? OR FUME# OR EFFLUV? OR EFFUS? OR EMISSION? OR EMANAT? OR OFFGAS##
L15 209185 SEA ETCH? OR PHOTOETCH? OR CHASE# OR CHASING# OR ENCHAS? OR ENGRAV? OR PHOTOENGRAV? OR EMBOSS? OR INCIS? OR IMPRINT? OR IMPRESS? OR ENCAUSTIC?
L16 24368 SEA FLUOROCARB? OR PERFLUOROCARB? OR FLUORCHEM? OR PERFLUOROCHEM? OR HYDROFLUOROCAR? OR HYDROFLUOROCHEM? OR FLUOROHYDROCARB? OR FLUOROHYDROCHEM? OR HFC#
L17 62922 SEA (CARRY OR CARRIER OR CARR? OR CONVEY? OR TRANSFER?)(3A)L14

FILE 'HCAPLUS' ENTERED AT 14:59:59 ON 10 APR 2002
L18 QUE SEMICOND? OR SEMI(A)(COND# OR CONDUCT?) OR IC OR ICS OR LCI OR I(W)C OR I(W)C(W)S OR VLSI# OR (INTEGRA? OR ELEC# OR ELECTRIC)(2A)CIRCUIT?
L19 QUE (TRANSISTOR? OR THYRISTOR? OR RECTIF? OR THYRECT? OR PHOTODIOD? OR PHOTOELEC? OR TRANSFORMER? OR SOLIDSTATE# OR (SOLID(2A)STATE#)(3A)(DEVICE? OR EQUIP?))
L20 QUE (PRINT? OR CIRCUIT? OR ELEC# OR ELECTRIC?)(2A)BOARD? OR (PRINT? OR ELEC# OR ELECTRIC?)(2A)WIR?(2A)BOARD? OR ((PWB# OR

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                MIB# OR PCB#) AND 76/SC,SX) OR (WIRE# OR WIRING#)(2A)HARNESS?
L21        446991 SEA (AR OR ARGON OR HE OR HELIUM OR XE OR XENON)

L22          3309 SEA (C3H2F6 OR HEXAFLUOROPROPANE OR C3F8 OR OCTAFLUOROPROPANE
                  OR PERFLUOROPROPANE OR C4H4F6 OR HEXAFLUOROBUTANE OR C4H2F8 OR
                  OCTAFLUOROBUTANE OR C5H4F8 OR OCTAFLUOROPENTANE)
L23             6 SEA (C3F6H2 OR C4F6H4 OR C4F8H2 OR C5F8H4)
L24          3312 SEA L22 OR L23

           FILE 'REGISTRY' ENTERED AT 15:31:34 ON 10 APR 2002
L25             1 SEA SILICON NITRIDE/CN
                  D L25
L26           356 SEA (SI(L)N)/ELS (L) 2/ELC.SUB
                  E SILICON OXIDE/CN
L27             2 SEA "SILICON OXIDE"/CN
                  D L27 1
L28           311 SEA (SI(L)O)/ELS (L) 2/ELC.SUB

                  E CH2F2/MF
L29            11 SEA CH2F2/MF
L30             1 SEA (C(L)H(L)F)/ELS (L) 3/ELC.SUB
                  E SILICON DIOXIDE
                  E SILICON DIOXIDE/CN
L31             1 SEA "SILICON DIOXIDE"/CN

            FILE 'HCAPLUS' ENTERED AT 15:56:35 ON 10 APR 2002
L32          1836 SEA L2 OR L3 OR L4 OR L5 OR L6
L33        150110 SEA L11 OR L12 OR L13
L34         68834 SEA L25 OR L26 OR (SILICON#(A)NITRIDE# OR SI3N4
L35        254311 SEA SIO OR SILICON(A)OXIDE OR SILICONOXIDE OR L27
L36        437937 SEA SIO2 OR SILICON(A)DIOXIDE# OR SILICONOXIDE# OR L27
L37        254532 SEA SIO OR SILICON(A)OXIDE# OR SILICONOXIDE# OR L27
L38          6697 SEA L28

L39        451784 SEA L21 OR L33
L40          3884 SEA L32 OR L22 OR L23
L41         14970 SEA L7 OR L8 OR TRIFLUOROMETHANE OR TRIFLUORO(A)METHANE OR
                  CHF3 OR CF3H OR PERFLUOROMETHANE OR TETRAFLUOROMETHANE OR
                  PERFLUORO(A)METHANE OR TETRAFLUORO(A)METHANE OR CF4
L42          1952 SEA DIFLUOROMETHANE OR CH2F2 OR CF2H2 OR DIFLUORO(A)METHANE
L43           125 SEA L40 AND L41 AND L42
L44            43 SEA L43 AND L15
L45            33 SEA L44 AND L18
L46            12 SEA L45 AND L39
L47            13 SEA L43 AND L39 AND L15
L48             4 SEA L47 AND L19
L49            23 SEA L43 AND L39
L50            13 SEA L49 AND L15
L51             0 SEA L50 AND L20

L52        450663 SEA L36 OR L37 OR L31 OR L28
L53         68834 SEA L25 OR L26 OR L34
L54        492200 SEA L52 OR L53
L55            27 SEA L43 AND L54 AND L15
L56            22 SEA L55 AND L18
L57             3 SEA L55 AND L19
L58             1 SEA L43 AND (L17(2A)L14) AND L54 AND L15
L59             6 SEA L43 AND (L17(2A)L14)
                  D SCAN
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L60          0 SEA L48 OR L57
L61          5 SEA L48 OR L57
L62         13 SEA L46 OR L47 OR L50
L63          9 SEA L62 NOT L61
L64         48 SEA L45 OR L49 OR L55 OR L56
L65         39 SEA L64 NOT L63


=> d L61 ibib abs hitind hitrn

L61  ANSWER 1 OF 5  HCAPLUS  COPYRIGHT 2002 ACS
ACCESSION NUMBER:         2002:51947  HCAPLUS
DOCUMENT NUMBER:          136:111232
TITLE:                    Method for forming a storage electrode on a
                          semiconductor device
INVENTOR(S):              Kim, Jeong Ho; Kim, Yu Chang
PATENT ASSIGNEE(S):       S. Korea
SOURCE:                   U.S. Pat. Appl. Publ., 9 pp.
                          CODEN: USXXCO
DOCUMENT TYPE:            Patent
LANGUAGE:                 English
FAMILY ACC. NUM. COUNT:   1
PATENT INFORMATION:

     PATENT NO.        KIND  DATE           APPLICATION NO.   DATE
     ---------------   ----  --------       ---------------   --------
     US 2002006697      A1   20020117       US 2001-860779    20010521
PRIORITY APPLN. INFO.:                     KR 2000-28008    A  20000524
AB   The present invention provides a method for forming a storage electrode on
     a semiconductor substrate, and in particular to a storage electrode
     formation method which can prevent formation of a sharp upper edged
     cylindrical storage electrode, thereby improving a dielec. property and
     reliability of a capacitor.
IC   ICM  H01L021-8238
NCL  438202000
CC   76-3 (Electric Phenomena)
IT   Capacitors
     Contact holes
     Dielectric films
     MOSFET (transistors)
     Semiconductor device fabrication
        (method for forming a storage electrode on a semiconductor device)
IT   7440-01-9, Neon, processes 7440-37-1, Argon, processes
     7440-59-7, Helium, processes 7440-63-3,
     Xenon, processes
     RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical
     process); PROC (Process); USES (Uses)
        (etching gas; method for forming a storage electrode on a
        semiconductor device)
IT   75-10-5, Difluoromethane 75-46-7, Fluoroform
     75-73-0, Carbon tetrafluoride 76-19-7, Octafluoropropane
     115-25-3, Octafluorocyclobutane  116-14-3, Tetrafluoroethene, processes
     124-38-9, Carbon dioxide, processes  559-40-0, Octafluorocyclopentene
     593-53-3, Monofluoromethane  630-08-0, Carbon monoxide, processes
     697-11-0, Hexafluorocyclobutene  2551-62-4, Sulfur hexafluoride
     7782-44-7, Oxygen, processes  7782-50-5, Chlorine, processes  7783-54-2,
     Nitrogen trifluoride  10035-10-6, Hydrogen bromide, processes
     10102-43-9, Nitrogen oxide (NO), processes  10102-44-0, Nitrogen oxide
     (NO2), processes  10294-34-5, Boron trichloride
```

RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(**etching** gas; method for forming a storage electrode on a semiconductor device)

IT 1314-61-0, Tantalum oxide 1344-28-1, Alumina, uses
RL: DEV (Device component use); USES (Uses)
(oxide **etch** barrier film; method for forming a storage electrode on a semiconductor device)

IT 7664-39-3, Hydrogen fluoride, processes 12125-01-8, Ammonium fluoride
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(wet **etching** soln.; method for forming a storage electrode on a semiconductor device)

IT **7440-37-1, Argon**, processes **7440-59-7, Helium**, processes **7440-63-3, Xenon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etching** gas; method for forming a storage electrode on a semiconductor device)

IT **75-46-7**, Fluoroform **76-19-7, Octafluoropropane**
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(**etching** gas; method for forming a storage electrode on a semiconductor device)

L61 ANSWER 2 OF 5 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:936069 HCAPLUS
DOCUMENT NUMBER: 136:62569
TITLE: Method for fabricating semiconductor device to prevent contact plug damage due to misalignment
INVENTOR(S): Kim, Jeong Ho; Kim, Yu Chang
PATENT ASSIGNEE(S): S. Korea
SOURCE: U.S. Pat. Appl. Publ., 8 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001055843	A1	20011227	US 2001-860769	20010521

PRIORITY APPLN. INFO.: KR 2000-28009 A 20000524

AB The present invention relates to a method semiconductor device fabrication for preventing or significantly reducing damage due to misalignment to active regions of a semiconductor substrate comprising a contact plug. In particular, methods of the present invention produces a contact plug which is larger than the presumed contact region. As a result, the acceptable process error margin for misalignment is increased, and the property and the yield of semiconductor devices are improved.

IC ICM H01L021-8238
NCL 438201000
CC 76-3 (Electric Phenomena)

IT **Etching**
MOSFET (**transistors**)
Photomasks (lithographic masks)
Semiconductor device fabrication
(method for fabricating semiconductor device to prevent contact plug damage due to misalignment)

IT 75-10-5, **Difluoromethane 75-46-7**, **Trifluoromethane** 75-73-0, **Tetrafluoromethane** **76-19-7**, **Octafluoropropane** 115-25-3, Octafluorocyclobutane 116-14-3, Tetrafluoroethene, processes 124-38-9, Carbon dioxide, processes 559-40-0, Octafluorocyclopentene 593-53-3, Fluoromethane 685-63-2, 1,3-Butadiene, 1,1,2,3,4,4-Hexafluoro- 931-91-9, Hexafluorocyclopropane 2551-62-4, Sulfur hexafluoride 7440-01-9, Neon, processes **7440-37-1**, **Argon**, processes **7440-59-7**, **Helium**, processes **7440-63-3**, **Xenon**, processes 7664-39-3, Hydrogen fluoride, processes 7664-93-9, Sulfuric acid, processes 7722-84-1, Hydrogen peroxide, processes 7782-50-5, Chlorine, processes 7783-54-2, Nitrogen trifluoride 10035-10-6, Hydrogen bromide, processes 10102-43-9, Nitric oxide, processes 10102-44-0, Nitrogen dioxide, processes 10294-34-5, Boron trichloride 12125-01-8, Ammonium fluoride
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating semiconductor device to prevent contact plug damage due to misalignment)

IT **75-46-7**, **Trifluoromethane** **76-19-7**, **Octafluoropropane** **7440-37-1**, **Argon**, processes **7440-59-7**, **Helium**, processes **7440-63-3**, **Xenon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating semiconductor device to prevent contact plug damage due to misalignment)

L61 ANSWER 3 OF 5 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:474233 HCAPLUS
DOCUMENT NUMBER: 135:69596
TITLE: Method for fabricating semiconductor device with a metal interconnection contact hole in a peripheral circuit region
INVENTOR(S): Kim, Jeong Ho; Kim, Yu Chang
PATENT ASSIGNEE(S): S. Korea
SOURCE: U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001005637	A1	20010628	US 2000-745429	20001226
US 6258722	B1	20010710	US 1999-473471	19991228
PRIORITY APPLN. INFO.:			KR 1999-61852 A	19991224

AB The present invention discloses a method for fabricating a semiconductor device. In a process for forming metal interconnection contact holes on both a gate electrode including an Si-rich SiON film as a mask insulating film in a peripheral circuit region and on a semiconductor substrate, the metal interconnection contact hole is formed according to a 3-step **etching** process using a photoresist film pattern exposing the intended locations of a metal interconnection contacts as an **etching** mask. Accordingly, contact properties are improved by preventing damage to the semiconductor substrate, thereby reducing leakage current and improving yield.
IC ICM H01L021-302
NCL 438710000

CC 76-3 (Electric Phenomena)
ST semiconductor device fabrication **etching** interconnection contact hole
IT Perfluorocarbons
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating semiconductor device with a metal interconnection contact hole in a peripheral circuit region)
IT Contact holes
Dielectric films
Electric insulators
Etching
Etching masks
Interconnections (electric)
MOSFET (**transistors**)
Photomasks (lithographic masks)
Semiconductor device fabrication
(method for fabricating semiconductor device with a metal interconnection contact hole in a peripheral circuit region)
IT 75-10-5, **Difluoromethane** **75-46-7**, **Trifluoromethane** 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane** 115-25-3, Octafluorocyclobutane 116-14-3, Tetrafluoroethene, processes 354-33-6, Pentafluoroethane 376-77-2, Decafluorocyclopentane 559-40-0, Octafluorocyclopentene 593-53-3, Fluoromethane 697-11-0, Hexafluorocyclobutene 931-91-9, Hexafluorocyclopropane 7783-54-2, Nitrogen trifluoride
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating semiconductor device with a metal interconnection contact hole in a peripheral circuit region)
IT 124-38-9, Carbon dioxide, processes 630-08-0, Carbon monoxide, processes 7440-01-9, Neon, processes **7440-37-1**, **Argon**, processes **7440-59-7**, **Helium**, processes **7440-63-3**, **Xenon**, processes 7782-44-7, Oxygen, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etching** mixt.; method for fabricating semiconductor device with a metal interconnection contact hole in a peripheral circuit region)
IT 7440-21-3, Silicon, uses 11105-01-4, **Silicon nitride** oxide **12033-89-5**, **Silicon nitride**, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(method for fabricating semiconductor device with a metal interconnection contact hole in a peripheral circuit region)
IT **75-46-7**, **Trifluoromethane** **76-19-7**, **Octafluoropropane**
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating semiconductor device with a metal interconnection contact hole in a peripheral circuit region)
IT **7440-37-1**, **Argon**, processes **7440-59-7**, **Helium**, processes **7440-63-3**, **Xenon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etching** mixt.; method for fabricating semiconductor device with a metal interconnection contact hole in a peripheral circuit region)
IT **12033-89-5**, **Silicon nitride**, uses

RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(method for fabricating semiconductor device with a metal interconnection contact hole in a peripheral circuit region)

L61 ANSWER 4 OF 5 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:474216 HCAPLUS
DOCUMENT NUMBER: 135:54527
TITLE: Semiconductor device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film
INVENTOR(S): Kim, Jeong Ho; Kim, Young Seo
PATENT ASSIGNEE(S): S. Korea
SOURCE: U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001005614	A1	20010628	US 2000-741879	20001222
US 6287905	B2	20010911		
JP 2001230387	A2	20010824	JP 2000-391917	20001225

PRIORITY APPLN. INFO.: KR 1999-61849 A 19991224

AB The present invention discloses a method for fabricating a semiconductor device. In a process for forming a bit line contact plug and storage electrode contact plug for the high integration semiconductor device, a MOSFET is formed, a device isolating insulating film protective film is formed at the upper portion of the resultant structure, a sacrificed insulating film pattern is formed at the upper portion of a contact region, an interlayer insulating film is formed and **etched** according to the CMP process to expose the sacrificed insulating film pattern, the device isolating insulating film protective film formed in the contact region is removed, and a contact plug is formed. That is, the **etching** process for exposing the contact region is performed on a device isolating insulating film, thereby preventing damage of the semiconductor substrate, improving a contact property, and restricting current leakage due to the damaged device isolating insulating film. Also, a margin for the misalignment is increased, and as a result device property and yield are improved.

IC ICM H01L021-336
NCL 438284000
CC 76-3 (Electric Phenomena)
IT Dielectric films
Etching
Integrated circuits
MOSFET (**transistors**)
Semiconductor device fabrication
(semiconductor device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)
IT 74-82-8, Methane, processes 74-85-1, Ethene, processes 74-86-2, Acetylene, processes 75-10-5, **Difluoromethane** **75-46-7**, **Trifluoromethane** 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane** 116-14-3, Tetrafluoroethene, processes 116-15-4, Hexafluoropropene 354-33-6, Pentafluoroethane 357-26-6, Octafluoro-1-butene 376-77-2, Decafluorocyclopentane 559-40-0, Octafluorocyclopentene 593-53-3, Fluoromethane 685-63-2, Hexafluoro-1,3-butadiene 1333-74-0, Hydrogen,

processes 1336-21-6, Ammonium hydroxide 2551-62-4, Sulfur hexafluoride 7664-39-3, Hydrogen fluoride, processes 7783-54-2, Nitrogen trifluoride
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; semiconductor device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT 409-21-2, Silicon carbide, uses 1314-61-0, Tantala 1344-28-1, Alumina, uses 7440-21-3, Silicon, uses 7440-33-7, Tungsten, uses 11105-01-4, **Silicon nitride** oxide **12033-89-5**, **Silicon nitride**, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(semiconductor device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT **75-46-7**, **Trifluoromethane 76-19-7**, **Octafluoropropane**
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; semiconductor device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT **12033-89-5**, **Silicon nitride**, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(semiconductor device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

L61 ANSWER 5 OF 5 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:293894 HCAPLUS
DOCUMENT NUMBER: 134:288911
TITLE: Anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication
INVENTOR(S): Boyd, D. C.; Boerns, S. M.; Hannafy, H. I.
PATENT ASSIGNEE(S): IBM Corp., USA
SOURCE: Faming Zhuanli Shenqing Gongkai Shuomingshu, 27 pp.
CODEN: CNXXEV
DOCUMENT TYPE: Patent
LANGUAGE: Chinese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
CN 1271871	A	20001101	CN 2000-106557	20000412
JP 2000340552	A2	20001208	JP 2000-124026	20000425

PRIORITY APPLN. INFO.: US 1999-299137 A 19990426

AB A technique for plasma anisotropic **etching silicon nitride** layer for manuf. of metal oxide semiconductor field-effect **transistor** is presented. The gas contains polymg. agent, H source, oxidizing agent, and rare gas dilg. agent. The polymg. agent is selected from **CF4**, C2F6, and **C3F8**. The H source is **CHF3**, **CH2F2**, CH3F, and H2. The oxidizing agent is CO, CO2, and O2. The novel gas dilg. agent is **He**, **Ar**, and Ne.

IC ICM G03F007-004
ICS G03F007-00

CC 76-3 (Electric Phenomena)

ST **silicon nitride** plasma **etching** field effect

transistor
IT MOSFET (**transistors**)
Sputtering
(anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)
IT **Etching**
(anisotropic; anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)
IT **Etching**
Vapor deposition process
(plasma; anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)
IT 78-10-4, TEOS
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(PECVD; anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)
IT **7631-86-9**, Silica, processes **12033-89-5**, **Silicon Nitride**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)
IT 75-10-5, **Difluoromethane** **75-46-7**, **Trifluoromethane** 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane** 124-38-9, Carbon dioxide, uses 593-53-3, Fluoromethane 630-08-0, Carbon monoxide, uses 1333-74-0, Hydrogen, uses 7440-01-9, Neon, uses **7440-37-1**, **Argon**, uses **7440-59-7**, **Helium**, uses 7782-44-7, Oxygen, uses
RL: NUU (Other use, unclassified); USES (Uses)
(plasma anisotropic **etchants**; anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)
IT **7631-86-9**, Silica, processes **12033-89-5**, **Silicon Nitride**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)
IT **75-46-7**, **Trifluoromethane** **76-19-7**, **Octafluoropropane** **7440-37-1**, **Argon**, uses **7440-59-7**, **Helium**, uses
RL: NUU (Other use, unclassified); USES (Uses)
(plasma anisotropic **etchants**; anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)

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L63 ANSWER 1 OF 9 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2002:193495 HCAPLUS
DOCUMENT NUMBER: 136:240060
TITLE: **Semiconductor** device fabrication by plasma **etching** of silicon oxide film using octafluorobutene gas and **semiconductor** device itself
INVENTOR(S): Kang, Chang Jin
PATENT ASSIGNEE(S): Samsung Electronics Co., Ltd., S. Korea

SOURCE: Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2002075975	A2	20020315	JP 2001-227553	20010727

PRIORITY APPLN. INFO.: KR 2000-50358 A 20000829

AB The title method involves using a plasma-**etching** gas contg. a linear unsatd. compd. of octafluorobutene. Specifically, the octafluorobutene may comprise octafluoro-1-butene or octafluoro-2-butene, and the silicon oxide film may comprises silica, borophosphosilicate glass, phosphosilicate glass, or silicon nitride oxide. Addnl., the **etching** gas may contain **CF4**, C2F6, C3F6, **C3F8**, C5F8, octafluorocyclobutane, **CHF3**, **CH2F2**, CH3F, **Ar**, **He**, Kr, **Xe**, or O2.

IC ICM H01L021-3065
ICS H01L021-28; H01L021-768

CC 76-3 (Electric Phenomena)

ST octafluorobutene plasma **etching** silica **semiconductor** device fabrication

IT **Etching**
(plasma; **semiconductor** device fabrication by plasma **etching** of silicon oxide film using fluorobutene gas and **semiconductor** device itself)

IT **Semiconductor** device fabrication
Semiconductor devices
(**semiconductor** device fabrication by plasma **etching** of silicon oxide film using fluorobutene gas and **semiconductor** device itself)

IT Borophosphosilicate glasses
Phosphosilicate glasses
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**semiconductor** device fabrication by plasma **etching** of silicon oxide film using fluorobutene gas and **semiconductor** device itself)

IT 7631-86-9, Silica, processes 11105-01-4, Silicon nitride oxide
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**semiconductor** device fabrication by plasma **etching** of silicon oxide film using fluorobutene gas and **semiconductor** device itself)

IT 75-10-5, **Difluoromethane** **75-46-7**, **Trifluoromethane** 75-73-0, Carbon fluoride (**CF4**) 76-16-4 **76-19-7** 115-25-3, Octafluorocyclobutane 116-15-4, Perfluoropropene 357-26-6, Octafluoro-1-butene 360-89-4, Octafluoro-2-butene 559-40-0, Perfluorocyclopentene 593-53-3, Methyl fluoride 7439-90-9, Krypton, uses **7440-37-1**, **Argon**, uses **7440-59-7**, **Helium**, uses **7440-63-3**, **Xenon**, uses 7782-44-7, Oxygen, uses
RL: NUU (Other use, unclassified); USES (Uses)
(**semiconductor** device fabrication by plasma **etching** of silicon oxide film using fluorobutene gas and **semiconductor** device itself)

IT **75-46-7**, **Trifluoromethane** **76-19-7** **7440-37-1**, **Argon**, uses **7440-59-7**,

Helium, uses **7440-63-3**, **Xenon**, uses
RL: NUU (Other use, unclassified); USES (Uses)
(**semiconductor** device fabrication by plasma **etching** of silicon oxide film using fluorobutene gas and **semiconductor** device itself)

L63 ANSWER 2 OF 9 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2002:11081 HCAPLUS
DOCUMENT NUMBER: 136:78346
TITLE: Fabrication method of **semiconductor integrated circuit** device
INVENTOR(S): Tadokoro, Masahiro; Shioya, Masahiro; Kojima, Masayuki; Ikeda, Takenobu
PATENT ASSIGNEE(S): Japan
SOURCE: U.S. Pat. Appl. Publ., 67 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002001963	A1	20020103	US 2001-893577	20010629
JP 2002025979	A2	20020125	JP 2000-200986	20000703

PRIORITY APPLN. INFO.: JP 2000-200986 A 20000703

AB A fabrication method of a **semiconductor integrated circuit** device comprises, in an SAC process or HARC process, subjecting a **semiconductor** substrate to plasma **etching** to make contact holes in an oxide film made of a Si oxide film formed on the **semiconductor** substrate. For improving the ease-in-**etching** property of the Si oxide film and selectivity to a nitride film, a residence time of an **etching** gas within a chamber is so set as to be in a range where selectivity to an insulating film made of Si nitride is improved by using **etching** conditions of a low pressure and a large flow rate of the **etching** gas of C5H8/O2/**Ar**.

IC ICM H01L021-302
ICS H01L021-461
NCL 438710000
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
ST manuf **semiconductor** device octafluorocyclopentane oxygen plasma **etching**
IT Ion implantation
(boron; fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)
IT Vapor deposition process
(chem., TEOS silica; fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)
IT Contact holes
Dielectric films
Integrated circuits
Semiconductor device fabrication
(fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)
IT **Etching**

(plasma; fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT Nitriding
(silica; fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT 7631-86-9, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(TEOS CVD; fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT 11105-01-4, Silicon nitride oxide
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT **7440-37-1, Argon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT 75-10-5, **Difluoromethane 75-46-7**, Fluoroform
75-73-0, Carbon tetrafluoride 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane** 115-25-3, Octafluorocyclobutane
593-53-3, Monofluoromethane 7782-44-7, Oxygen, processes 139064-01-0, Octafluorocyclopentane
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT 7440-42-8, Boron, uses
RL: MOA (Modifier or additive use); USES (Uses)
(ion implantation; fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT 7440-33-7, Tungsten, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(metal film; fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT 7664-41-7, Ammonia, processes 10102-43-9, Nitrogen oxide (NO), processes
10102-44-0, Nitrogen oxide (NO2), processes
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(nitriding silica; fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT 7440-21-3, Silicon, processes

RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst. lower electrode; fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT 78-10-4, TEOS
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(silica CVD; fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT **7440-37-1**, **Argon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

IT **75-46-7**, Fluoroform **76-19-7**, **Octafluoropropane**
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(fabrication method of **semiconductor integrated circuit** device using C5F8/O2/**Ar** as plasma **etching** gases)

L63 ANSWER 3 OF 9 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:924301 HCAPLUS
DOCUMENT NUMBER: 136:46929
TITLE: Method for forming a silicide gate stack for use in a self-aligned contact **etch**
INVENTOR(S): Hineman, Max F.
PATENT ASSIGNEE(S): Hineman, Max, USA
SOURCE: U.S. Pat. Appl. Publ., 14 pp., Division of U.S. Ser. No. 533,697.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001053595	A1	20011220	US 2001-901036	20010710
WO 2001071800	A3	20020307	WO 2001-US9054	20010322

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

PRIORITY APPLN. INFO.: US 2000-533697 A3 20000323

AB A method for forming a gate stack having a silicide layer that can subsequently undergo a SAC **etch** is disclosed. The present method provides a layer of insulating material on top of the silicide layer. The insulating material is sufficient to protect the gate stack, including the silicide layer when the low-resistance gate stack is used in subsequent self-aligned contact **etch** processes.

IC ICM H01L021-3205
NCL 438592000
CC 76-3 (Electric Phenomena)
ST **semiconductor** device fabrication silicide gate stack self aligned contact
IT Dielectric films
Electric insulators
Etching
Semiconductor device fabrication
(method for forming a silicide gate stack for use in a self-aligned contact **etch**)
IT Borophosphosilicate glasses
Borosilicate glasses
Phosphosilicate glasses
RL: DEV (Device component use); USES (Uses)
(method for forming a silicide gate stack for use in a self-aligned contact **etch**)
IT Electric contacts
(self-aligned; method for forming a silicide gate stack for use in a self-aligned contact **etch**)
IT Silicides
RL: DEV (Device component use); USES (Uses)
(self-aligned; method for forming a silicide gate stack for use in a self-aligned contact **etch**)
IT **Etching**
(sputter, ion-beam, reactive; method for forming a silicide gate stack for use in a self-aligned contact **etch**)
IT 7439-98-7, Molybdenum, uses 7440-06-4, Platinum, uses 7440-25-7, Tantalum, uses 7440-32-6, Titanium, uses 7440-33-7, Tungsten, uses 7440-48-4, Cobalt, uses
RL: DEV (Device component use); USES (Uses)
(device suicide layer; method for forming a silicide gate stack for use in a self-aligned contact **etch**)
IT 74-82-8, Methane, processes 75-10-5, **Difluoromethane** **75-46-7, Trifluoromethane** 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane** 106-97-8, Butane, processes 354-33-6, Pentafluoroethane 593-53-3, Fluoromethane **7440-37-1**, **Argon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(**etchant**; method for forming a silicide gate stack for use in a self-aligned contact **etch**)
IT 78-10-4, Tetraethoxysilane 7631-86-9, Silica, uses 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(method for forming a silicide gate stack for use in a self-aligned contact **etch**)
IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(polycryst.; method for forming a silicide gate stack for use in a self-aligned contact **etch**)
IT **75-46-7, Trifluoromethane 76-19-7, Octafluoropropane 7440-37-1, Argon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(**etchant**; method for forming a silicide gate stack for use in a self-aligned contact **etch**)

L63 ANSWER 4 OF 9 HCAPLUS COPYRIGHT 2002 ACS

ACCESSION NUMBER: 2001:874623 HCAPLUS
DOCUMENT NUMBER: 136:13954
TITLE: Method of forming dual damascene structure with improved contact/via edge integrity
INVENTOR(S): Tsai, Chia Shiung; Tao, Hun-jan
PATENT ASSIGNEE(S): Taiwan Semiconductor Manufacturing Company, Taiwan
SOURCE: U.S., 10 pp.
CODEN: USXXAM
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6326296	B1	20011204	US 1998-108867	19980701

AB A new method of forming a dual damascene interconnect is disclosed for manufg. **semiconductor** substrates. A contact/via hole is 1st formed in a 1st dielec. layer formed over a substructure of a substrate having devices formed therein and/or metal layers formed thereon. The contact/via hole is filled with a protective material prior to forming a 2nd dielec. layer. Conductive line opening is formed in the 2nd dielec. layer and over the contact/via hole having the protective material in it. The protective material protects the edge of the contact/via hole from damage due to the 2nd **etching** of the conductive line opening. Thus, a dual damascene structure is disclosed wherein the integrity of the edge of the contact/via hole is preserved, avoiding any reliability problems in the **semiconductor** product.

IC ICM H01L021-4763
NCL 438624000
CC 76-2 (Electric Phenomena)
IT Antireflective films
Contact holes
Dielectric films
Etching
Photolithography
(in forming dual damascene structure with improved contact/via edge integrity)
IT **Etching**
Vapor deposition process
(plasma; in forming dual damascene structure with improved contact/via edge integrity)
IT 11105-01-4, Silicon nitride oxide 12033-89-5, Silicon nitride (Si3N4), processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etch** stop; in forming dual damascene structure with improved contact/via edge integrity)
IT **7440-59-7, Helium**, uses
RL: NUU (Other use, unclassified); USES (Uses)
(plasma carrier gas; in forming dual damascene structure with improved contact/via edge integrity)
IT 7782-44-7, Oxygen, uses
RL: NUU (Other use, unclassified); USES (Uses)
(plasma **etchant**; in forming dual damascene structure with improved contact/via edge integrity)
IT 75-10-5, **Difluoromethane 75-46-7, Trifluoromethane** 75-73-0, **Tetrafluoromethane 76-19-7, Perfluoropropane** 115-25-3, Perfluorocyclobutane **7440-37-1, Argon**, processes

RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(plasma **etchant**; in forming dual damascene structure with improved contact/via edge integrity)

IT **7440-59-7, Helium**, uses
RL: NUU (Other use, unclassified); USES (Uses)
(plasma carrier gas; in forming dual damascene structure with improved contact/via edge integrity)

IT **75-46-7, Trifluoromethane 76-19-7, Perfluoropropane 7440-37-1, Argon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(plasma **etchant**; in forming dual damascene structure with improved contact/via edge integrity)

REFERENCE COUNT: 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L63 ANSWER 5 OF 9 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:474223 HCAPLUS
DOCUMENT NUMBER: 135:54532
TITLE: Method for fabricating **semiconductor** device
INVENTOR(S): Kim, Jeong Ho; Yu, Jae Seon
PATENT ASSIGNEE(S): S. Korea
SOURCE: U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001005626	A1	20010628	US 2000-741878	20001222

PRIORITY APPLN. INFO.: KR 1999-61846 A 19991224

AB The present invention discloses a method for fabricating a **semiconductor** device. A protective film for protecting a device isolation film is formed on the device isolation film for the contact hole formation process, preventing a device isolation film from being damaged due to misalignment in a lithog. process or overetch during the **etch** process. Gate induced drain leakage current is not generated, contact junction leakage current is reduced, and the contact properties are improved. Improvements in the contact properties produce corresponding improvements in the properties and yield of the **semiconductor** devices manufd. according to the invention.

IC ICM H01L021-4763
NCL 438637000
CC 76-3 (Electric Phenomena)
ST **semiconductor** device fabrication
IT Polishing
(chem.-mech.; in fabricating **semiconductor** device)
IT **Etching**
Lithography
(in fabricating **semiconductor** device)
IT **Semiconductor** device fabrication
(method for)
IT 409-21-2, Silicon monocarbide, uses 39345-87-4, Silicon carbide oxide
RL: NUU (Other use, unclassified); USES (Uses)
(hydrogenated; **semiconductor** device protective film using)
IT 7440-21-3, Silicon, uses 7440-32-6, Titanium, uses 7440-33-7, Tungsten, uses 25583-20-4, Titanium mononitride

RL: DEV (Device component use); USES (Uses)
(**semiconductor** device contact plug using)
IT 74-82-8, Methane, processes 74-85-1, Ethene, processes 75-10-5, **Difluoromethane 75-46-7**, Fluoroform 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane** 116-14-3, Tetrafluoroethene, processes 116-15-4, Hexafluoropropene 354-33-6, Pentafluoroethane 593-53-3, Fluoromethane 685-63-2 1333-74-0, Hydrogen, processes 2465-56-7, Methylene **7440-37-1**, **Argon**, processes 7782-44-7, Oxygen, processes 11070-66-9, Octafluorobutene 12693-22-0, Pentene, decafluoro- 72923-38-7, Pentadiene, octafluoro-
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(**semiconductor** device protective film **etched** using)
IT 1314-61-0, Tantalum pentoxide 1344-28-1, Alumina, uses 11105-01-4, Silicon nitride oxide 12033-89-5, Silicon nitride, uses
RL: NUU (Other use, unclassified); USES (Uses)
(**semiconductor** device protective film using)
IT 7664-38-2, Phosphoric acid, processes
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(**semiconductor** device protective film wet **etched** using)
IT **75-46-7**, Fluoroform **76-19-7**, **Octafluoropropane** **7440-37-1**, **Argon**, processes
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(**semiconductor** device protective film **etched** using)

L63 ANSWER 6 OF 9 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:210341 HCAPLUS
DOCUMENT NUMBER: 134:230802
TITLE: Apparatus and method for plasma processing
INVENTOR(S): Yokokawa, Katanobu; Izawa, Masaru; Itabashi, Naoshi; Yamamoto, Seiji; Taji, Shinichi; Negishi, Nobuyuki; Takahashi, Nushito
PATENT ASSIGNEE(S): Hitachi, Ltd., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001077090	A2	20010323	JP 1999-249639	19990903

AB The title method involves forming a plasma by the interaction between an electromagnetic wave of 300-500 MHz and a magnetic field, applying an electromagnetic wave of 50-30 MHz on an electromagnetic-wave-introduction plate while superimposing on the electromagnetic wave of 300-500 MHz, and maintaining a certain spacing between the plate and substrate to be processed. The active species in the plasma are effectively controlled independent from the plasma-generation conditions for stable processing for a long period of time. An app. for carrying out the above method is also described. The method and app. are useful for plasma **etching** of an insulator film in **semiconductor** device fabrication.
IC ICM H01L021-3065
ICS C23F004-00; H01L021-31
CC 76-11 (Electric Phenomena)

ST plasma processing app **semiconductor** device fabrication
IT Dielectric films
Electric discharge devices
Etching apparatus
Semiconductor device fabrication
(app. and method for plasma processing)
IT **Etching**
(plasma; app. and method for plasma processing)
IT 64-17-5, Ethanol, uses 67-56-1, Methanol, uses 67-66-3, Trichloromethane, uses 74-82-8, Methane, uses 75-10-5, **Difluoromethane 75-46-7, Trifluoromethane** 76-16-4, Perfluoroethane **76-19-7, Perfluoropropane** 115-25-3, Perfluorocyclobutane 116-14-3, Tetrafluoroethylene, uses 116-15-4, Perfluoropropene 593-53-3, Fluoromethane 630-08-0, Carbon monoxide, uses 684-16-2, Perfluoroacetone 1333-74-0, Hydrogen, uses 2314-97-8, Iodotrifluoromethane 2551-62-4, Sulfur hexafluoride **7440-37-1, Argon,** uses 7647-01-0, Hydrogen chloride, uses 7664-41-7, Ammonia, uses 7727-37-9, Nitrogen, uses 7782-44-7, Oxygen, uses 7782-50-5, Chlorine, uses 7783-54-2, Nitrogen trifluoride 10035-10-6, Hydrogen bromide, uses 10294-34-5, Boron trichloride
RL: NUU (Other use, unclassified); USES (Uses)
(app. and method for plasma processing)
IT **75-46-7, Trifluoromethane 76-19-7, Perfluoropropane 7440-37-1, Argon,** uses
RL: NUU (Other use, unclassified); USES (Uses)
(app. and method for plasma processing)

L63 ANSWER 7 OF 9 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2000:723625 HCAPLUS
DOCUMENT NUMBER: 133:289914
TITLE: Manufacture of **semiconductor** device by dry **etching** with mixing gas for low emission of perfluorocarbons
INVENTOR(S): Sato, Masayuki
PATENT ASSIGNEE(S): Nec Corp., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000286241	A2	20001013	JP 1999-90903	19990331

AB A Si3N4 film is **etched** by plasma using a mixing gas contg. a fluorocarbon gas, a given additive gas, etc., (e.g., **CHF3** + MeOH + **He**). The **etching** rate is improved (e.g., 120 nm/min), because the C and H atoms in the MeOH additive gas bond with the N atoms in the Si3N4 film and C-N and N-H bonds are generated. The mixing gas doesn't **etch** an oxide film because the MeOH additive gas doesn't react with an oxide film.
IC ICM H01L021-3065
ICS H01L021-28; H01L029-78
CC 76-3 (Electric Phenomena)
ST gas dry **etching semiconductor** device manuf; silicon nitride film plasma **etching** gas; fluorocarbon additive mixing gas dry **etching**
IT Hydrocarbons, uses
RL: NUU (Other use, unclassified); USES (Uses)

(fluoro, mixing gas components; manuf. of **semiconductor** device by dry **etching** with mixing gas for low emission of perfluorocarbons)

IT **Semiconductor** device fabrication
(manuf. of **semiconductor** device by dry **etching** with mixing gas for low emission of perfluorocarbons)

IT **Etching**
(plasma; manuf. of **semiconductor** device by dry **etching** with mixing gas for low emission of perfluorocarbons)

IT 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(manuf. of **semiconductor** device by dry **etching** with mixing gas for low emission of perfluorocarbons)

IT 64-17-5, Ethanol, uses 67-56-1, Methanol, uses 74-82-8, Methane, uses 74-83-9, Methyl bromide, uses 75-10-5, **Difluoromethane** **75-46-7, Trifluoromethane** 75-73-0, **Tetrafluoromethane** 593-53-3, Monofluoromethane 1333-74-0, Hydrogen, uses **7440-59-7, Helium**, uses **26447-60-9, Octafluorobutane**
RL: NUU (Other use, unclassified); USES (Uses)
(mixing gas component; manuf. of **semiconductor** device by dry **etching** with mixing gas for low emission of perfluorocarbons)

IT **75-46-7, Trifluoromethane 7440-59-7, Helium**, uses **26447-60-9, Octafluorobutane**
RL: NUU (Other use, unclassified); USES (Uses)
(mixing gas component; manuf. of **semiconductor** device by dry **etching** with mixing gas for low emission of perfluorocarbons)

L63 ANSWER 8 OF 9 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1999:687661 HCAPLUS
DOCUMENT NUMBER: 132:29254
TITLE: New contact **etch** process for embedded DRAM applications
AUTHOR(S): Yang, Chan-Lon; Chen, Tong-Yu; Huang, Keh-Ching; Jung, Le-Tien; Lin, Tsu-An; Lur, Water
CORPORATE SOURCE: United Microelectronics Corporation, Hsinchu, Taiwan
SOURCE: Materials Research Society Symposium Proceedings (1999), 564(Advanced Interconnects and Contacts), 177-182
CODEN: MRSPDH; ISSN: 0272-9172
PUBLISHER: Materials Research Society
DOCUMENT TYPE: Journal
LANGUAGE: English

AB For embedded DRAM (E-DRAM) devices with feature sizes of 0.25 .mu.m and beyond, contact processes with low contact resistance and low junction leakage current are required. The contact **etch** process needs to **etch** through multi-layer structures with SiO2, SiON/SiN layers and stop on Ti-polycide gate and Ti-salicide active regions at the same time. The key issues include high selectivity to TiSix, vertical profile, complete removal of SiON/SiN cap layer and no polymer residues. In this paper, multi-layer contact **etching** without attacking TiSix is reported. Using new process chem., the new contact **etch** process has been demonstrated for the manufg. of 0.25 .mu.m E-DRAM and beyond.

CC 76-3 (Electric Phenomena)

ST plasma **etching** silicon DRAM contact

IT Memory devices
(DRAM (dynamic random access); contact **etch** process for embedded DRAM applications)

IT Contact resistance

Leakage current
(contact **etch** process for embedded DRAM applications)
IT Polymers, uses
RL: DEV (Device component use); FMU (Formation, unclassified); FORM (Formation, nonpreparative); USES (Uses)
(contact **etch** process for embedded DRAM applications)
IT **Etching**
(plasma; contact **etch** process for embedded DRAM applications)
IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes 11105-01-4, Silicon nitride oxide 12033-89-5, Silicon nitride, processes 12738-91-9, Titanium silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(contact **etch** process for embedded DRAM applications)
IT 75-10-5, **Difluoromethane 75-46-7**, **Trifluoromethane** 115-25-3, Perfluoro-cyclobutane 593-53-3, Fluoromethane 630-08-0, Carbon monoxide, processes **7440-37-1**, **Argon**, processes **27070-61-7**, **Hexafluoropropane** 29759-38-4, Tetrafluoroethane
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(**etchant**; contact **etch** process for embedded DRAM applications)
IT **75-46-7**, **Trifluoromethane 7440-37-1**, **Argon**, processes **27070-61-7**, **Hexafluoropropane**
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(**etchant**; contact **etch** process for embedded DRAM applications)
REFERENCE COUNT: 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L63 ANSWER 9 OF 9 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1997:664840 HCAPLUS
DOCUMENT NUMBER: 127:364536
TITLE: Highly selective SiO2 **etch** employing inductively coupled hydro-fluorocarbon plasma chemistry for self aligned contact **etch**
AUTHOR(S): Iijima, Yukio; Ishikawa, Yoshio; Yang, Chan-lon; Chang, Mei; Okano, Haruo
CORPORATE SOURCE: Applied Materials Japan Inc., Chiba, 286, Japan
SOURCE: Jpn. J. Appl. Phys., Part 1 (1997), 36(9A), 5498-5501
CODEN: JAPNDE; ISSN: 0021-4922
PUBLISHER: Japanese Journal of Applied Physics
DOCUMENT TYPE: Journal
LANGUAGE: English
AB An inductively coupled plasma chem. including hydrofluorocarbon gas (**CHF3**, **CH2F2** or CH3F) in addn. to C4F8 and **Ar** was developed for the self aligned contact process of LSI. The addnl. gases effectively reduces the **etch** rate of the nitride stopper in the contact hole resulting an increased selective ratio. The effect becomes more marked with higher H nos. The optical emission signals of both F radical and C, including radicals such as C2, CF and CF2, were decreased by the addn. of CH3F. The improved selectivity is considered to be due to the increased concn. of radicals with C-H bonding. The effect of C-H including radicals was explained by the enthalpy of reaction with O and N atoms to form CO or CN bonding, and an improved step coverage of the polymd. film protecting the nitride surface.
CC 76-3 (Electric Phenomena)
ST contact hole silica selective plasma **etching**; hydrofluorocarbon plasma **etching** silica contact hole
IT Contact holes

Semiconductor device fabrication
(highly selective silica **etch** employing inductively coupled hydrofluorocarbon plasma chem. for self aligned contact **etch** with silicon nitride stopper)

IT Sputter **etching** kinetics
(of nitride stopper in contact hole)

IT Radicals, formation (nonpreparative)
RL: FMU (Formation, unclassified); FORM (Formation, nonpreparative)
(radical formation in hydrofluorocarbon **etchant** plasma)

IT Sputter **etching**
(selective; highly selective silica **etch** employing inductively coupled hydrofluorocarbon plasma chem. for self aligned contact **etch** with silicon nitride stopper)

IT Selective **etching**
(sputter; highly selective silica **etch** employing inductively coupled hydrofluorocarbon plasma chem. for self aligned contact **etch** with silicon nitride stopper)

IT 7631-86-9, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(highly selective silica **etch** employing inductively coupled hydrofluorocarbon plasma chem. for self aligned contact **etch** with silicon nitride stopper)

IT 75-10-5, **Difluoromethane** **75-46-7**, **Trifluoromethane** 76-16-4, Perfluoroethane **76-19-7**, **Perfluoropropane** 115-25-3, Perfluorocyclobutane 593-53-3, Monofluoromethane **7440-37-1**, **Argon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(highly selective silica **etch** employing inductively coupled hydrofluorocarbon plasma chem. for self aligned contact **etch** with silicon nitride stopper)

IT 12033-89-5, Silicon nitride, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(highly selective silica **etch** employing inductively coupled hydrofluorocarbon plasma chem. for self aligned contact **etch** with silicon nitride stopper)

IT 2154-59-8, Carbon difluoride 3889-75-6, Carbon fluoride (CF) 12070-15-4, Carbon dimer
RL: FMU (Formation, unclassified); FORM (Formation, nonpreparative)
(radical formation in hydrofluorocarbon **etchant** plasma)

IT **75-46-7**, **Trifluoromethane** **76-19-7**, **Perfluoropropane** **7440-37-1**, **Argon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(highly selective silica **etch** employing inductively coupled hydrofluorocarbon plasma chem. for self aligned contact **etch** with silicon nitride stopper)

=> d L65 1-39 ti

L65 ANSWER 1 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Method for forming a storage electrode on a **semiconductor** device

L65 ANSWER 2 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Self-aligned contact (SAC) **etch** with dual-chemistry process

L65 ANSWER 3 OF 39 HCAPLUS COPYRIGHT 2002 ACS

TI Plasma **etching** of **semiconductor** wafers having stable resist pattern to promote high aspect ratio

L65 ANSWER 4 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment

L65 ANSWER 5 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region

L65 ANSWER 6 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Method for fabricating **semiconductor** device with a pad polycrystalline silicon layer and a contact plug grown by selective epitaxy

L65 ANSWER 7 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI **Semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film

L65 ANSWER 8 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication

L65 ANSWER 9 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Treatment after comprehensive **etching** following dielectric **etching** of **semiconductor** structure

L65 ANSWER 10 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Treatment of **semiconductor** structures after dielectric layer **etching**

L65 ANSWER 11 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Dry **etching** and **semiconductor** device fabrication

L65 ANSWER 12 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Process and apparatus for recovery of valuable components from waste gases in **semiconductor** manufacturing

L65 ANSWER 13 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Fabrication of magnetic thin film recording head by reactive ion beam **etching**

L65 ANSWER 14 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Variable load refrigeration system particularly for cryogenic temperatures

L65 ANSWER 15 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI **Etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** with a high-density plasma **etcher**

L65 ANSWER 16 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Microwave-activated plasma **etching** of dielectric layers

L65 ANSWER 17 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Fabrication of **semiconductor** devices in prevention of particle contamination from plasma **etching** chamber

L65 ANSWER 18 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Anisotropic selective **etching** of nitride of multilayer structure

in high-density plasma for high aspect ratio application

L65 ANSWER 19 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Acoustically active drug delivery systems comprising a gas or gaseous precursor filled microsphere

L65 ANSWER 20 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Preparation of solid porous matrixes for pharmaceutical uses

L65 ANSWER 21 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Undoped **silicon dioxide** as an **etch** stop for selective **etching** of doped **silicon dioxide**

L65 ANSWER 22 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Gas and gaseous precursor filled microspheres as topical and subcutaneous delivery vehicles

L65 ANSWER 23 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Process and installation for the treatment of perfluorinated and hydrofluorocarbon gases, for the purpose of their destruction

L65 ANSWER 24 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Anisotropic dry **etching** of borophosphosilicate glasses in high selectivity

L65 ANSWER 25 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Preparation of perfluorocarbons.

L65 ANSWER 26 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Plasma **etching** of oxide with high selectivity to nitride suitable for use on surfaces of uneven topography

L65 ANSWER 27 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Manufacture of **semiconductor** device by dry-**etching**

L65 ANSWER 28 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Manufacture of **semiconductor** devices

L65 ANSWER 29 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Dry **etching** of **silicon oxide** film for manufacture of **semiconductor** device

L65 ANSWER 30 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Plasma **etching** of oxide in the presence of nitride

L65 ANSWER 31 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI **Etching** of electric insulator films for **semiconductor** devices

L65 ANSWER 32 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI **Semiconductor** devices and their manufacture

L65 ANSWER 33 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Therapeutic delivery systems comprising gas precursor-filled microspheres

L65 ANSWER 34 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Dry **etching**

L65 ANSWER 35 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Method for selectively **etching** a III-V **semiconductor**,

in the production of a field-effect transistor

L65 ANSWER 36 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Gaseous ultrasound contrast media and method for selecting gases for use as ultrasound contrast media

L65 ANSWER 37 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI On the UV and visible emission bands of trifluoromethyl radicals produced by pulsed electron beam excitation

L65 ANSWER 38 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Determination of thermal conductivity, accomodation coefficient, and free convection of 40 gases with a thermistor bridge and with the thin wire-capillary method

L65 ANSWER 39 OF 39 HCAPLUS COPYRIGHT 2002 ACS
TI Action of elementary fluorine upon organic compounds. IX. The vapor phase fluorination of methane

=> d L65 1-13,15-18,21,24,26-32,34-35 ibib abs hitind hitrn

L65 ANSWER 1 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2002:51947 HCAPLUS
DOCUMENT NUMBER: 136:111232
TITLE: Method for forming a storage electrode on a **semiconductor** device
INVENTOR(S): Kim, Jeong Ho; Kim, Yu Chang
PATENT ASSIGNEE(S): S. Korea
SOURCE: U.S. Pat. Appl. Publ., 9 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002006697	A1	20020117	US 2001-860779	20010521

PRIORITY APPLN. INFO.: KR 2000-28008 A 20000524

AB The present invention provides a method for forming a storage electrode on a **semiconductor** substrate, and in particular to a storage electrode formation method which can prevent formation of a sharp upper edged cylindrical storage electrode, thereby improving a dielec. property and reliability of a capacitor.

IC ICM H01L021-8238
NCL 438202000
CC 76-3 (Electric Phenomena)
ST storage electrode **semiconductor** device
IT Polishing
(chem.-mech.; method for forming a storage electrode on a **semiconductor** device)
IT Films
(elec. conductive, polysilicon; method for forming a storage electrode on a **semiconductor** device)
IT Electric conductors
(films, polysilicon; method for forming a storage electrode on a **semiconductor** device)
IT Capacitors
Contact holes

Dielectric films
MOSFET (transistors)
Semiconductor device fabrication
(method for forming a storage electrode on a **semiconductor** device)

IT 7440-01-9, Neon, processes **7440-37-1, Argon**, processes **7440-59-7, Helium**, processes **7440-63-3, Xenon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etching** gas; method for forming a storage electrode on a **semiconductor** device)

IT 75-10-5, **Difluoromethane 75-46-7**, Fluoroform
75-73-0, Carbon tetrafluoride **76-19-7, Octafluoropropane**
115-25-3, Octafluorocyclobutane 116-14-3, Tetrafluoroethene, processes
124-38-9, Carbon dioxide, processes 559-40-0, Octafluorocyclopentene
593-53-3, Monofluoromethane 630-08-0, Carbon monoxide, processes
697-11-0, Hexafluorocyclobutene 2551-62-4, Sulfur hexafluoride
7782-44-7, Oxygen, processes 7782-50-5, Chlorine, processes 7783-54-2, Nitrogen trifluoride 10035-10-6, Hydrogen bromide, processes
10102-43-9, Nitrogen oxide (NO), processes 10102-44-0, Nitrogen oxide (NO2), processes 10294-34-5, Boron trichloride
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(**etching** gas; method for forming a storage electrode on a **semiconductor** device)

IT 1314-61-0, Tantalum oxide 1344-28-1, Alumina, uses
RL: DEV (Device component use); USES (Uses)
(oxide **etch** barrier film; method for forming a storage electrode on a **semiconductor** device)

IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(polycryst. conductive film; method for forming a storage electrode on a **semiconductor** device)

IT 7664-39-3, Hydrogen fluoride, processes 12125-01-8, Ammonium fluoride
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(wet **etching** soln.; method for forming a storage electrode on a **semiconductor** device)

IT **7440-37-1, Argon**, processes **7440-59-7, Helium**, processes **7440-63-3, Xenon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etching** gas; method for forming a storage electrode on a **semiconductor** device)

IT **75-46-7**, Fluoroform **76-19-7, Octafluoropropane**
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(**etching** gas; method for forming a storage electrode on a **semiconductor** device)

L65 ANSWER 2 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2002:23838 HCAPLUS
DOCUMENT NUMBER: 136:94482
TITLE: Self-aligned contact (SAC) **etch** with dual-chemistry process
INVENTOR(S): Ko, Kei-yu
PATENT ASSIGNEE(S): Micron Technology, Inc., USA
SOURCE: U.S., 10 pp.
CODEN: USXXAM

DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6337285	B1	20020108	US 2000-532088	20000321

AB The invention is a two-step dual-chem. process for **etching** through a selected portion of an insulating oxide layer of a substrate to create a self-aligned contact opening without damaging underlying field oxide regions. The first **etching** step uses essentially a CxFy (x>1)-type chem. that **etches** only partially through the oxide layer, since it has very good selectivity to the **silicon nitride** cap of the gate stacks but a poor selectivity to the field oxide regions. The second **etching** step employs a second chem. comprising an H-contg. fluorocarbon chem. The second chem. has a good selectivity to the field oxide regions and, at the same time, is able to finish **etching** the opening.

IC ICM H01L021-302
ICS B44C001-22; C03C015-00

NCL 438714000

CC 76-3 (Electric Phenomena)

ST selfaligned contact **etch** dual chem process

IT Memory devices
(DRAM (dynamic random access), fabrication of; self-aligned contact **etch** with dual-chem. process for)

IT Sputtering
(**etching**, reactive; self-aligned contact **etch** with dual-chem. process for)

IT **Etching**
(plasma; self-aligned contact **etch** with dual-chem. process for)

IT Electric contacts
Electric insulators
Etching
Interconnections (electric)
(self-aligned contact **etch** with dual-chem. process)

IT MOS devices
SOI devices
Semiconductor device fabrication
(self-aligned contact **etch** with dual-chem. process for)

IT Borosilicate glasses
Phosphosilicate glasses
RL: DEV (Device component use); USES (Uses)
(self-aligned contact **etch** with dual-chem. process for)

IT Borophosphosilicate glasses
RL: DEV (Device component use); PRP (Properties); PRP (Properties); USES (Uses)
(self-aligned contact **etch** with dual-chem. process for)

IT **Etching**
(sputter, reactive; self-aligned contact **etch** with dual-chem. process for)

IT 1317-82-4, Sapphire 7440-21-3, Silicon, uses **12033-89-5**, **Silicon nitride**, uses 12627-41-7, Tungsten silicide
RL: DEV (Device component use); USES (Uses)
(self-aligned contact **etch** with dual-chem. process for)

IT 75-10-5, **Difluoromethane 75-46-7**, **Trifluoromethane** 76-16-4, Perfluoroethane **76-19-7**, **Perfluoropropane** 115-25-3, Perfluorocyclobutane 116-14-3,

Perfluoroethene, uses 355-25-9, Perfluorobutane 559-40-0, Perfluorocyclopentene
RL: NUU (Other use, unclassified); USES (Uses)
(self-aligned contact **etch** with dual-chem. process for)
IT **12033-89-5, Silicon nitride**, uses
RL: DEV (Device component use); USES (Uses)
(self-aligned contact **etch** with dual-chem. process for)
IT **75-46-7, Trifluoromethane 76-19-7, Perfluoropropane**
RL: NUU (Other use, unclassified); USES (Uses)
(self-aligned contact **etch** with dual-chem. process for)
REFERENCE COUNT: 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L65 ANSWER 3 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2002:10909 HCAPLUS
DOCUMENT NUMBER: 136:78281
TITLE: Plasma **etching** of **semiconductor** wafers having stable resist pattern to promote high aspect ratio
INVENTOR(S): Donohoe, Kevin G.; Stocks, Rich
PATENT ASSIGNEE(S): Micron Technology, Inc., USA
SOURCE: U.S. Pat. Appl. Publ., 12 pp., Division of U.S. Ser. No. 342,677.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002000422	A1	20020103	US 2001-916734	20010726

PRIORITY APPLN. INFO.: US 1999-342677 A3 19990629
AB The Si-**semiconductor** or similar oxide surface is precoated with a patterned resist layer, and is then exposed for plasma **etching** of the bare area, during which the resist thickness is increased, or is **etched** at a rate .gtoreq.10 times slower than that of the bare area. The plasma is generated from the gas mixt. contg. fluorinated hydrocarbon gases (esp. **CH2F2**), typically using RF excitation at 1-3 MHz. The initial **etching** without resist removal is optionally followed by conventional plasma **etching**. By combining the initial **etching** that increases the resist thickness with the subsequent **etching** of the resist, the **elec.-circuit** conductor features can be **etched** to have high aspect ratio for increased depth.
IC ICM C23F001-00
ICS C23F003-00; B44C001-22
NCL 216064000
CC 76-3 (Electric Phenomena)
ST **semiconductor** wafer plasma **etching** resist pattern; flurocarbon gas plasma **etching** silicon wafer resist
IT **Integrated circuits**
(**etching** of; plasma **etching** of **semiconductors** with stable resist pattern for high aspect ratio)
IT Resists
(films; plasma **etching** of **semiconductors** with stable resist pattern for high aspect ratio)
IT Hydrocarbons, uses

RL: MOA (Modifier or additive use); USES (Uses)
(fluoro, gas, plasma with; plasma **etching** of **semiconductors** with stable resist pattern for high aspect ratio)

IT **Etching**
(plasma, on **semiconductors**; plasma **etching** of **semiconductors** with stable resist pattern for high aspect ratio)

IT **7631-86-9**, Silica, processes
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); PROC (Process)
(film, **etching** of; plasma **etching** of Si **semiconductors** with stable resist pattern for high aspect ratio)

IT 75-10-5, **Difluoromethane** **75-46-7**, **Trifluoromethane** 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7**, Propane, octafluoro- 354-33-6, Ethane, pentafluoro- 593-53-3, Monofluoromethane
RL: MOA (Modifier or additive use); USES (Uses)
(plasma with; plasma **etching** of Si **semiconductors** with stable resist pattern for high aspect ratio)

IT 7440-21-3, Silicon, processes
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); PROC (Process)
(**semiconductor**, **etching** of; plasma **etching** of Si **semiconductors** with stable resist pattern for high aspect ratio)

IT **7631-86-9**, Silica, processes
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); PROC (Process)
(film, **etching** of; plasma **etching** of Si **semiconductors** with stable resist pattern for high aspect ratio)

IT **75-46-7**, **Trifluoromethane** **76-19-7**, Propane, octafluoro-
RL: MOA (Modifier or additive use); USES (Uses)
(plasma with; plasma **etching** of Si **semiconductors** with stable resist pattern for high aspect ratio)

L65 ANSWER 4 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:936069 HCAPLUS
DOCUMENT NUMBER: 136:62569
TITLE: Method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment
INVENTOR(S): Kim, Jeong Ho; Kim, Yu Chang
PATENT ASSIGNEE(S): S. Korea
SOURCE: U.S. Pat. Appl. Publ., 8 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001055843	A1	20011227	US 2001-860769	20010521

PRIORITY APPLN. INFO.: KR 2000-28009 A 20000524

AB The present invention relates to a method **semiconductor** device fabrication for preventing or significantly reducing damage due to misalignment to active regions of a **semiconductor** substrate

comprising a contact plug. In particular, methods of the present invention produces a contact plug which is larger than the presumed contact region. As a result, the acceptable process error margin for misalignment is increased, and the property and the yield of **semiconductor** devices are improved.

IC ICM H01L021-8238
NCL 438201000
CC 76-3 (Electric Phenomena)
ST **semiconductor** device fabrication contact plug misalignment damage prevention
IT Films
(elec. conductive; method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment)
IT Electric conductors
(films; method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment)
IT Electric insulators
(isolation; method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment)
IT **Etching**
MOSFET (transistors)
Photomasks (lithographic masks)
Semiconductor device fabrication
(method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment)
IT Electric contacts
(plugs; method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment)
IT 75-10-5, **Difluoromethane 75-46-7**, **Trifluoromethane** 75-73-0, **Tetrafluoromethane 76-19-7**, **Octafluoropropane** 115-25-3, Octafluorocyclobutane 116-14-3, Tetrafluoroethene, processes 124-38-9, Carbon dioxide, processes 559-40-0, Octafluorocyclopentene 593-53-3, Fluoromethane 685-63-2, 1,3-Butadiene, 1,1,2,3,4,4-Hexafluoro-931-91-9, Hexafluorocyclopropane 2551-62-4, Sulfur hexafluoride 7440-01-9, Neon, processes **7440-37-1**, **Argon**, processes **7440-59-7**, **Helium**, processes **7440-63-3**, **Xenon**, processes 7664-39-3, Hydrogen fluoride, processes 7664-93-9, Sulfuric acid, processes 7722-84-1, Hydrogen peroxide, processes 7782-50-5, Chlorine, processes 7783-54-2, Nitrogen trifluoride 10035-10-6, Hydrogen bromide, processes 10102-43-9, Nitric oxide, processes 10102-44-0, Nitrogen dioxide, processes 10294-34-5, Boron trichloride 12125-01-8, Ammonium fluoride
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment)
IT 1314-61-0, Tantala 1344-28-1, Alumina, uses 7429-90-5, Aluminum, uses 25583-20-4, Titanium nitride (TiN)
RL: DEV (Device component use); USES (Uses)
(method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment)
IT 7440-25-7, Tantalum, uses 7440-32-6, Titanium, uses 7440-33-7, Tungsten, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment)
IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); TEM (Technical or engineered material

use); USES (Uses)
(polycryst.; method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment)
IT **75-46-7, Trifluoromethane 76-19-7, Octafluoropropane 7440-37-1, Argon**, processes **7440-59-7, Helium**, processes **7440-63-3, Xenon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating **semiconductor** device to prevent contact plug damage due to misalignment)

L65 ANSWER 5 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:474233 HCAPLUS
DOCUMENT NUMBER: 135:69596
TITLE: Method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region
INVENTOR(S): Kim, Jeong Ho; Kim, Yu Chang
PATENT ASSIGNEE(S): S. Korea
SOURCE: U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001005637	A1	20010628	US 2000-745429	20001226
US 6258722	B1	20010710	US 1999-473471	19991228
PRIORITY APPLN. INFO.:			KR 1999-61852 A	19991224

AB The present invention discloses a method for fabricating a **semiconductor** device. In a process for forming metal interconnection contact holes on both a gate electrode including an Si-rich SiON film as a mask insulating film in a peripheral circuit region and on a **semiconductor** substrate, the metal interconnection contact hole is formed according to a 3-step **etching** process using a photoresist film pattern exposing the intended locations of a metal interconnection contacts as an **etching** mask. Accordingly, contact properties are improved by preventing damage to the **semiconductor** substrate, thereby reducing leakage current and improving yield.
IC ICM H01L021-302
NCL 438710000
CC 76-3 (Electric Phenomena)
ST **semiconductor** device fabrication **etching** interconnection contact hole
IT **Semiconductor** devices
(electrodes; method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region)
IT Perfluorocarbons
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region)
IT Contact holes
Dielectric films
Electric insulators

Etching
Etching masks
Interconnections (electric)
MOSFET (transistors)
Photomasks (lithographic masks)
Semiconductor device fabrication
(method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region)

IT Electric contacts
(plugs; method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region)

IT Electrodes
(**semiconductive**; method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region)

IT 75-10-5, **Difluoromethane** **75-46-7**, **Trifluoromethane** 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane** 115-25-3, Octafluorocyclobutane 116-14-3, Tetrafluoroethene, processes 354-33-6, Pentafluoroethane 376-77-2, Decafluorocyclopentane 559-40-0, Octafluorocyclopentene 593-53-3, Fluoromethane 697-11-0, Hexafluorocyclobutene 931-91-9, Hexafluorocyclopropane 7783-54-2, Nitrogen trifluoride
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region)

IT 124-38-9, Carbon dioxide, processes 630-08-0, Carbon monoxide, processes 7440-01-9, Neon, processes **7440-37-1**, **Argon**, processes **7440-59-7**, **Helium**, processes **7440-63-3**, **Xenon**, processes 7782-44-7, Oxygen, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etching** mixt.; method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region)

IT 7440-21-3, Silicon, uses 11105-01-4, **Silicon nitride** oxide **12033-89-5**, **Silicon nitride**, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region)

IT **75-46-7**, **Trifluoromethane** **76-19-7**, **Octafluoropropane**
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region)

IT **7440-37-1**, **Argon**, processes **7440-59-7**, **Helium**, processes **7440-63-3**, **Xenon**, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etching** mixt.; method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region)

IT **12033-89-5**, **Silicon nitride**, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)

(method for fabricating **semiconductor** device with a metal interconnection contact hole in a peripheral circuit region)

L65 ANSWER 6 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:474221 HCAPLUS
DOCUMENT NUMBER: 135:54530
TITLE: Method for fabricating **semiconductor** device with a pad polycrystalline silicon layer and a contact plug grown by selective epitaxy
INVENTOR(S): Kim, Jeong Ho; Kim, Yu Chang
PATENT ASSIGNEE(S): Kim, Jeong, S. Korea
SOURCE: U.S. Pat. Appl. Publ., 8 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001005623	A1	20010628	US 2000-741880	20001222
PRIORITY APPLN. INFO.:			KR 1999-61848 A	19991224

AB The present invention discloses a method for fabricating a **semiconductor** device. In a process for forming a contact plug, a pad polycryst. Si layer pattern is formed at the presumed contact region, and a contact plug is formed according to a selective epitaxial growth (SEG) method using the pad polycryst. Si layer pattern as a seed. Accordingly, a higher contact plug is formed by improving a growth rate of the SEG process, and thus a succeeding process can be easily performed. In the SEG process, a contact property is improved by compensating for a **semiconductor** substrate damaged in a process for forming an insulating film spacer at the sidewalls of a gate electrode. As a result, the property and yield of the **semiconductor** device are remarkably improved.

IC ICM H01L021-336
ICS H01L021-8234; H01L021-44; H01L021-302; H01L021-461
NCL 438597000
CC 76-3 (Electric Phenomena)
ST **semiconductor** device fabrication contact plug selective epitaxy
IT Electric insulators
(isolation; method for fabricating **semiconductor** device with a pad polycryst. silicon layer and a contact plug grown by selective epitaxy)
IT Contact holes
Dielectric films
Etching
Etching masks
Semiconductor device fabrication
(method for fabricating **semiconductor** device with a pad polycryst. silicon layer and a contact plug grown by selective epitaxy)
IT Electric contacts
(plugs; method for fabricating **semiconductor** device with a pad polycryst. silicon layer and a contact plug grown by selective epitaxy)
IT Epitaxy
(selective; method for fabricating **semiconductor** device with a pad polycryst. silicon layer and a contact plug grown by selective epitaxy)
IT 74-82-8, Methane, processes 74-85-1, Ethene, processes 74-86-2, Acetylene, processes 75-10-5, **Difluoromethane 75-46-7**

, **Trifluoromethane** 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7, Octafluoropropane** 116-14-3, Tetrafluoroethene, processes 116-15-4, Hexafluoropropene 354-33-6, Pentafluoroethane 357-26-6, Octafluoro-1-butene 376-77-2, Decafluorocyclopentane 559-40-0, Octafluorocyclopentene 593-53-3, Fluoromethane 685-63-2, Hexafluoro-1,3-butadiene 1333-74-0, Hydrogen, processes 2551-62-4, Sulfur hexafluoride 7783-54-2, Nitrogen trifluoride
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating **semiconductor** device with a pad polycryst. silicon layer and a contact plug grown by selective epitaxy)

IT **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(method for fabricating **semiconductor** device with a pad polycryst. silicon layer and a contact plug grown by selective epitaxy)

IT 1314-61-0, Tantala 1344-28-1, Alumina, uses 11105-01-4, **Silicon nitride** oxide **12033-89-5**, **Silicon nitride**, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(method for fabricating **semiconductor** device with a pad polycryst. silicon layer and a contact plug grown by selective epitaxy)

IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(polycryst.; method for fabricating **semiconductor** device with a pad polycryst. silicon layer and a contact plug grown by selective epitaxy)

IT **75-46-7, Trifluoromethane 76-19-7, Octafluoropropane**
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; method for fabricating **semiconductor** device with a pad polycryst. silicon layer and a contact plug grown by selective epitaxy)

IT **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(method for fabricating **semiconductor** device with a pad polycryst. silicon layer and a contact plug grown by selective epitaxy)

IT **12033-89-5, Silicon nitride**, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(method for fabricating **semiconductor** device with a pad polycryst. silicon layer and a contact plug grown by selective epitaxy)

L65 ANSWER 7 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:474216 HCAPLUS
DOCUMENT NUMBER: 135:54527
TITLE: **Semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film
INVENTOR(S): Kim, Jeong Ho; Kim, Young Seo
PATENT ASSIGNEE(S): S. Korea
SOURCE: U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001005614	A1	20010628	US 2000-741879	20001222
US 6287905	B2	20010911		
JP 2001230387	A2	20010824	JP 2000-391917	20001225

PRIORITY APPLN. INFO.: KR 1999-61849 A 19991224

AB The present invention discloses a method for fabricating a **semiconductor** device. In a process for forming a bit line contact plug and storage electrode contact plug for the high integration **semiconductor** device, a MOSFET is formed, a device isolating insulating film protective film is formed at the upper portion of the resultant structure, a sacrificed insulating film pattern is formed at the upper portion of a contact region, an interlayer insulating film is formed and **etched** according to the CMP process to expose the sacrificed insulating film pattern, the device isolating insulating film protective film formed in the contact region is removed, and a contact plug is formed. That is, the **etching** process for exposing the contact region is performed on a device isolating insulating film, thereby preventing damage of the **semiconductor** substrate, improving a contact property, and restricting current leakage due to the damaged device isolating insulating film. Also, a margin for the misalignment is increased, and as a result device property and yield are improved.

IC ICM H01L021-336

NCL 438284000

CC 76-3 (Electric Phenomena)

ST **semiconductor** device fabrication plug contact isolation

IT Polishing
(chem.-mech.; **semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT Silicate glasses
RL: TEM (Technical or engineered material use); USES (Uses)
(device dielec. layer; **semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT Electric insulators
(isolation; **semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT Electric contacts
(plugs; **semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT Epitaxy
(selective; **semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT Dielectric films
Etching
Integrated circuits
MOSFET (transistors)
Semiconductor device fabrication
(**semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT Borophosphosilicate glasses
Phosphosilicate glasses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)

(**semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT 78-10-4, Tetraethoxysilane
RL: TEM (Technical or engineered material use); USES (Uses)
(device dielec. layer; **semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT 74-82-8, Methane, processes 74-85-1, Ethene, processes 74-86-2, Acetylene, processes 75-10-5, **Difluoromethane 75-46-7**, **Trifluoromethane** 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7, Octafluoropropane** 116-14-3, Tetrafluoroethene, processes 116-15-4, Hexafluoropropene 354-33-6, Pentafluoroethane 357-26-6, Octafluoro-1-butene 376-77-2, Decafluorocyclopentane 559-40-0, Octafluorocyclopentene 593-53-3, Fluoromethane 685-63-2, Hexafluoro-1,3-butadiene 1333-74-0, Hydrogen, processes 1336-21-6, Ammonium hydroxide 2551-62-4, Sulfur hexafluoride 7664-39-3, Hydrogen fluoride, processes 7783-54-2, Nitrogen trifluoride
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; **semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT 409-21-2, Silicon carbide, uses 1314-61-0, Tantala 1344-28-1, Alumina, uses 7440-21-3, Silicon, uses 7440-33-7, Tungsten, uses 11105-01-4, **Silicon nitride** oxide **12033-89-5**, **Silicon nitride**, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(**semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT **75-46-7, Trifluoromethane 76-19-7, Octafluoropropane**
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant**; **semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

IT **12033-89-5, Silicon nitride**, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(**semiconductor** device fabrication method for forming bit line and storage electrode contacts without damaging a device isolation film)

L65 ANSWER 8 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:293894 HCAPLUS
DOCUMENT NUMBER: 134:288911
TITLE: Anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication
INVENTOR(S): Boyd, D. C.; Boerns, S. M.; Hannafy, H. I.
PATENT ASSIGNEE(S): IBM Corp., USA
SOURCE: Faming Zhuanli Shenqing Gongkai Shuomingshu, 27 pp.
CODEN: CNXXEV
DOCUMENT TYPE: Patent
LANGUAGE: Chinese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
CN 1271871	A	20001101	CN 2000-106557	20000412
JP 2000340552	A2	20001208	JP 2000-124026	20000425

PRIORITY APPLN. INFO.: US 1999-299137 A 19990426

AB A technique for plasma anisotropic **etching silicon nitride** layer for manuf. of metal oxide **semiconductor** field-effect transistor is presented. The gas contains polymg. agent, H source, oxidizing agent, and rare gas dilg. agent. The polymg. agent is selected from **CF4**, C2F6, and **C3F8**. The H source is **CHF3**, **CH2F2**, CH3F, and H2. The oxidizing agent is CO, CO2, and O2. The novel gas dilg. agent is **He**, **Ar**, and Ne.

IC ICM G03F007-004
ICS G03F007-00

CC 76-3 (Electric Phenomena)

ST **silicon nitride** plasma **etching** field effect transistor

IT MOSFET (transistors)
Sputtering
(anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)

IT **Etching**
(anisotropic; anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)

IT **Etching**
Vapor deposition process
(plasma; anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)

IT 78-10-4, TEOS
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(PECVD; anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)

IT **7631-86-9**, Silica, processes **12033-89-5**, **Silicon Nitride**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)

IT 75-10-5, **Difluoromethane** **75-46-7**, **Trifluoromethane** 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane** 124-38-9, Carbon dioxide, uses 593-53-3, Fluoromethane 630-08-0, Carbon monoxide, uses 1333-74-0, Hydrogen, uses 7440-01-9, Neon, uses **7440-37-1**, **Argon**, uses **7440-59-7**, **Helium**, uses 7782-44-7, Oxygen, uses
RL: NUU (Other use, unclassified); USES (Uses)
(plasma anisotropic **etchants**; anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)

IT **7631-86-9**, Silica, processes **12033-89-5**, **Silicon Nitride**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)

IT **75-46-7**, **Trifluoromethane** **76-19-7**, **Octafluoropropane** **7440-37-1**, **Argon**, uses

7440-59-7, **Helium**, uses
RL: NUU (Other use, unclassified); USES (Uses)
(plasma anisotropic **etchants**; anisotropic **etching** technique for **silicon nitride** layer in MOSFET fabrication)

L65 ANSWER 9 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:31097 HCAPLUS
DOCUMENT NUMBER: 134:94341
TITLE: Treatment after comprehensive **etching** following dielectric **etching** of **semiconductor** structure
INVENTOR(S): Hui, Oh Yan; Yang, Chih Pin; Lin, Yei; Wu, Robert; Chen, Chih Pan; Chen, Yu Nen; Yang, Chan-Lon; Chen, Tong Yu
PATENT ASSIGNEE(S): Applied Materials, Inc., USA
SOURCE: Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 2
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001007094	A2	20010112	JP 2000-134003	20000502
PRIORITY APPLN. INFO.:			US 1999-304449 A	19990503
			US 1999-320251 A	19990526

AB The title treatment is conducted on a **semiconductor** structure consisting of an upper patterned photoresist layer, **etched** dielec. layer disposed under the patterned photoresist layer, an antireflective layer disposed below the dielec. layer, and a conductive layer disposed below the antireflective layer. The **semiconductor** structure is exposed to plasma obtained from a source gas consisting of O,N -contg. gas, and a reactive gas consisting of H, C, and F (e.g., **CHF3**, **CH2F2**, CH3F, C3H2H6, or H and C2F6, C3F6, **C3F8**, C4F6, C4F8).
IC ICM H01L021-3065
ICS H01L021-28; H01L021-768
CC 76-3 (Electric Phenomena)
ST **semiconductor** structure dielec **etching** aftertreatment plasma
IT Plasma
(in treatment after comprehensive **etching** following dielec. **etching** of **semiconductor** structure)
IT Electric insulators
Etching
Semiconductor devices
(treatment after comprehensive **etching** following dielec. **etching** of **semiconductor** structure)
IT 7429-90-5, Aluminum, uses 25583-20-4, Titanium nitride
RL: NUU (Other use, unclassified); USES (Uses)
(conductive layer; treatment after comprehensive **etching** following dielec. **etching** of **semiconductor** structure)
IT 75-10-5, **Difluoromethane 75-46-7**, **Trifluoromethane** 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane** 116-15-4, Hexafluoropropene 593-53-3, Monofluoromethane 1333-74-0, Hydrogen, uses 7727-37-9, Nitrogen, uses 7782-44-7, Oxygen, uses 11070-66-9, OctafluoroButene **27070-61-7**

, **Hexafluoropropane**
RL: NUU (Other use, unclassified); USES (Uses)
(plasma of gas contg.; in treatment after comprehensive **etching** following dielec. **etching** of **semiconductor** structure)
IT **75-46-7, Trifluoromethane 76-19-7, Octafluoropropane 27070-61-7, Hexafluoropropane**
RL: NUU (Other use, unclassified); USES (Uses)
(plasma of gas contg.; in treatment after comprehensive **etching** following dielec. **etching** of **semiconductor** structure)

L65 ANSWER 10 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2001:31096 HCAPLUS
DOCUMENT NUMBER: 134:94340
TITLE: Treatment of **semiconductor** structures after dielectric layer **etching**
INVENTOR(S): Hui, Ou Yang; Yang, Chi Ping; Ye, Ling; Wu, Robert; Chien, Chi Pang; Chien, Yu Neng
PATENT ASSIGNEE(S): Applied Materials, Inc., USA
SOURCE: Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 2
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001007093	A2	20010112	JP 2000-134002	20000502
PRIORITY APPLN. INFO.:			US 1999-304449 A	19990503

AB In the title treatment, the **semiconductor** structure is exposed to plasma obtained by using a source gas contg. O, N-contg. gas, and a reactive gas consisting of H, C, and F. Examples of the reactive gas include **CHF3**, **CH2F2**, CH3F, **C3H2F6**, C3F6, **C3F8**, C4F6, C4F8. Side wall shape is improved.
IC ICM H01L021-3065
ICS H01L021-28; H01L021-768
CC 76-3 (Electric Phenomena)
ST **semiconductor** structure dielec **etching** aftertreatment plasma fluorine
IT Electric insulators
Etching
Semiconductor device fabrication
(treatment of **semiconductor** structures after dielec. layer **etching**)
IT 75-10-5, **Difluoromethane 75-46-7, Trifluoromethane 76-19-7, Octafluoropropane** 116-15-4, Hexafluoropropene 593-53-3, Monofluoromethane 685-63-2 7727-37-9, Nitrogen, uses 7782-44-7, Oxygen, uses 11070-66-9, Octafluorobutene **27070-61-7, Hexafluoropropane**
RL: NUU (Other use, unclassified); USES (Uses)
(treatment of **semiconductor** structures after dielec. layer **etching** with plasma obtained using)
IT **75-46-7, Trifluoromethane 76-19-7, Octafluoropropane 27070-61-7, Hexafluoropropane**
RL: NUU (Other use, unclassified); USES (Uses)
(treatment of **semiconductor** structures after dielec. layer **etching** with plasma obtained using)

L65 ANSWER 11 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2000:880791 HCAPLUS
DOCUMENT NUMBER: 134:50093
TITLE: Dry **etching** and **semiconductor** device fabrication
INVENTOR(S): Yamanaka, Michinari; Kato, Junichi; Hori, Atsushi; Ogura, Masaki
PATENT ASSIGNEE(S): Matsushita Electric Industrial Co., Ltd., Japan; Halo LSI Design and Device Technology Inc.
SOURCE: Jpn. Kokai Tokkyo Koho, 15 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000349074	A2	20001215	JP 1999-161928	19990609

AB A method for fabricating a **semiconductor** device involves forming a gate electrode on a Si substrate having a gate insulator film, depositing a polysilicon film to cover the gate electrode, covering the polysilicon film at one side of the gate electrode, and chem. dry **etching** the polysilicon film exposed at the other side at a high **etching** rate and then at a low **etching** rate but at a high selectivity to prevent the gate insulator film from being damaged. Specifically, an O **etching** gas may be used, which contains **CF4**, **CHF3**, **CH2F2**, CH3F, C2F6, **C3F8**, C4F8, NF3 and/or SF6 (or HBr, Br2, Cl2, HCl, SiCl4, and/or BCl3).
IC ICM H01L021-3065
ICS H01L027-115; H01L021-8247; H01L029-788; H01L029-792
CC 76-3 (Electric Phenomena)
ST dry **etching** silicon **semiconductor** device fabrication
IT **Semiconductor** device fabrication
(dry **etching** of silicon and **semiconductor** device fabrication)
IT **Etching**
(dry; dry **etching** of silicon and **semiconductor** device fabrication)
IT 75-10-5, **Difluoromethane 75-46-7**, **Trifluoromethane** 75-73-0, Carbon fluoride (**CF4**) 76-16-4 **76-19-7** 115-25-3, Perfluorocyclobutane 593-53-3, Methyl fluoride 2551-62-4, Sulfur fluoride (SF6) 7647-01-0, Hydrogen chloride, uses 7726-95-6, Bromine, uses 7782-44-7, Oxygen, uses 7782-50-5, Chlorine, uses 7783-54-2, Nitrogen fluoride (NF3) 10026-04-7, Silicon chloride (SiCl4) 10035-10-6, Hydrogen bromide, uses 10294-34-5, Boron chloride (BCl3)
RL: NUU (Other use, unclassified); USES (Uses)
(dry **etching** of silicon and **semiconductor** device fabrication)
IT 7440-21-3, Silicon, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(dry **etching** of silicon and **semiconductor** device fabrication)
IT **75-46-7**, **Trifluoromethane 76-19-7**
RL: NUU (Other use, unclassified); USES (Uses)
(dry **etching** of silicon and **semiconductor** device fabrication)

L65 ANSWER 12 OF 39 HCAPLUS COPYRIGHT 2002 ACS

ACCESSION NUMBER: 2000:847801 HCAPLUS
DOCUMENT NUMBER: 134:8583
TITLE: Process and apparatus for recovery of valuable components from waste gases in **semiconductor** manufacturing
INVENTOR(S): Shitara, Chiharu
PATENT ASSIGNEE(S): NEC Corp., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000334258	A2	20001205	JP 1999-145291	19990525

AB The title process comprises dilg. a waste gas from **semiconductor** manufg. by a gas having b.p. higher than the highest b.p. (Bp) of valuable components in the waste gas, and keeping the dild. waste gas at a temp. lower than b.p. of the dilg. gas and also higher than Bp for recovery of the dilg. gas as a liq. and the valuable components as gases. Alternatively, the temp. of the dild. waste gas is kept higher than the second highest b.p. of the valuable components. The process may contain removing impurities before recovery of the valuable components. The valuable components may contain fluoro(hydro)carbons, N fluorides, and/or S fluorides. The dilg. gases may contain CF3CF2CF3, cyclic C4F8, CF3CFCF2, CH2FCF3, CHF2CF3, MeCHF2, and/or **CH2F2**. The title app. contains the mixing step, a remover to remove impurities, and the collecting tower. The valuable components are recovered as gases at low cost from waste gases in dry **etching** or CVD process for **semiconductor** manufg.

IC ICM B01D053-34
ICS B01D053-46; F25J003-06; H01L021-3065; H01L021-31
CC 59-4 (Air Pollution and Industrial Hygiene)
Section cross-reference(s): 47, 76
ST waste gas fluorocarbon recovery **semiconductor** manufg
IT Vapor deposition process
(chem.; control of temp. in dilg. and cooling in recovery of fluoro compd. from waste gas of **semiconductor** manufg. by dry **etching** and CVD)
IT **Semiconductor** device fabrication
Waste gases
(control of temp. in dilg. and cooling in recovery of fluoro compd. from waste gas of **semiconductor** manufg. by dry **etching** and CVD)
IT **Etching**
(dry; control of temp. in dilg. and cooling in recovery of fluoro compd. from waste gas of **semiconductor** manufg. by dry **etching** and CVD)
IT Hydrocarbons, uses
RL: NUU (Other use, unclassified); PUR (Purification or recovery); PREP (Preparation); USES (Uses)
(fluoro; control of temp. in dilg. and cooling in recovery of fluoro compd. from waste gas of **semiconductor** manufg. by dry **etching** and CVD)
IT **75-46-7P, Trifluoromethane** 75-73-0P, Carbon tetrafluoride 76-16-4P, Hexafluoroethane 2551-62-4P, Sulfur hexafluoride 7783-54-2P, Nitrogen trifluoride
RL: PUR (Purification or recovery); PREP (Preparation)

(control of temp. in dilg. and cooling in recovery of fluoro compd. from waste gas of **semiconductor** manufg. by dry **etching** and CVD)

IT 75-10-5, **Difluoromethane** 75-37-6, 1,1-Difluoroethane **76-19-7, Perfluoropropane** 116-15-4, Perfluoropropene 287-23-0, Cyclobutane 354-33-6, Pentafluoroethane 754-12-1, 2,3,3,3-Tetrafluoropropene
RL: NUU (Other use, unclassified); USES (Uses)
(dilg. gases; control of temp. in dilg. and cooling in recovery of fluoro compd. from waste gas of **semiconductor** manufg. by dry **etching** and CVD)

IT **75-46-7P, Trifluoromethane**
RL: PUR (Purification or recovery); PREP (Preparation)
(control of temp. in dilg. and cooling in recovery of fluoro compd. from waste gas of **semiconductor** manufg. by dry **etching** and CVD)

IT **76-19-7, Perfluoropropane**
RL: NUU (Other use, unclassified); USES (Uses)
(dilg. gases; control of temp. in dilg. and cooling in recovery of fluoro compd. from waste gas of **semiconductor** manufg. by dry **etching** and CVD)

L65 ANSWER 13 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2000:707387 HCAPLUS
DOCUMENT NUMBER: 133:275472
TITLE: Fabrication of magnetic thin film recording head by reactive ion beam **etching**
INVENTOR(S): Williams, Kurt E.; Druz, Boris L.; Hines, Danielle S.; Londono, John F.
PATENT ASSIGNEE(S): Veeco Instruments, Inc., USA
SOURCE: PCT Int. Appl., 42 pp.
CODEN: PIXXD2
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2000058953	A2	20001005	WO 2000-US8400	20000330
WO 2000058953	A3	20010426		
W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
RW: GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				
US 6238582	B1	20010529	US 1999-281663	19990330
EP 1183684	A2	20020306	EP 2000-919854	20000330
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				

PRIORITY APPLN. INFO.: US 1999-281663 A 19990330
WO 2000-US8400 W 20000330

AB A reactive ion beam **etching** method which employs an oxidizing agent in a plasma contained in an ion source to control carbonaceous deposit (e.g., polymer) formation within the ion source and on the substrate. During operation of an ion source, after operating the ion

source with a plasma having a carbonaceous deposit forming species, a plasma contg. an oxidizing agent (species) is generated within the ion source. Preferably, within the ion source a plasma is maintained essentially continuously between the time that the carbonaceous deposit forming species is present and the time that the oxidizing agent is present. A reactive ion beam extd. from an ion source contg. a plasma having an oxidizing species may be impinged onto a sample substrate to remove (i.e., **etch**) any carbonaceous material deposit (e.g., polymers) formed on the sample, such as may be formed from previous reactive ion beam **etching** (RIBE) processing steps using an ion beam having species which may form carbonaceous (e.g., polymer) deposits on the sample substrate structure. Preferably, a reactive ion beam contg. an oxidizing species is incident upon the sample at an angle which enhances the selectivity of the carbonaceous deposit (e.g., polymer) **etching** relative to other materials upon which the ion beam impinges. A thin film magnetic head is fabricated according to a pole trimming process which employs RIBE with an oxidizing species to remove any carbonaceous material (e.g., polymer) deposits formed during a previous fluorocarbon based RIBE step.

IC ICM G11B005-31
ICS C23F004-00

CC 77-8 (Magnetic Phenomena)
Section cross-reference(s): 38, 76

ST reactive ion beam **etching** polymer magnetic film recording head; oxidizing agent carbonaceous material fluorocarbon **etching** **semiconductor** device fabrication

IT Sputtering
(**etching**, ion-beam, reactive; fabrication of magnetic thin film recording head by)

IT Hydrocarbons, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fluoro, plasma; in reative ion-beam **etching** fabrication of magnetic thin film recording head)

IT Hydrocarbons, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(halo, precursors; in reative ion-beam **etching** fabrication of magnetic thin film recording head)

IT Magnetic films
(in reative ion-beam **etching** fabrication of magnetic recording head)

IT Electric contacts
Electric insulators
Ferroelectric materials
Oxidizing agents
Photolithography
Photomasks (lithographic masks)
Photoresists
Semiconductor materials
(in reative ion-beam **etching** fabrication of magnetic thin film recording head)

IT Polyimides, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in reative ion-beam **etching** fabrication of magnetic thin film recording head)

IT Carbonaceous materials (technological products)
Polymers, processes
RL: NUU (Other use, unclassified); OCU (Occurrence, unclassified); PEP

(Physical, engineering or chemical process); OCCU (Occurrence); PROC (Process); USES (Uses)
(in reative ion-beam **etching** fabrication of magnetic thin film recording head)

IT Magnetic recording heads
(reative ion-beam **etching** fabrication of)

IT **Etching**
(reative ion-beam **etching** fabrication of magnetic thin film recording head)

IT Electrodeposition
(selective; in reative ion-beam **etching** fabrication of magnetic thin film recording head)

IT **Etching**
(selective; reative ion-beam **etching** fabrication of magnetic thin film recording head)

IT **Etching**
(sputter, ion-beam, reactive; fabrication of magnetic thin film recording head by)

IT 1303-00-0, Gallium arsenide, processes 1344-28-1, Alumina, processes 7439-89-6, Iron, processes 7439-96-5, Manganese, processes 7440-02-0, Nickel, processes 7440-21-3, Silicon, processes 7440-32-6, Titanium, processes 7440-33-7, Tungsten, processes 7440-47-3, Chromium, processes 7440-48-4, Cobalt, processes **7631-86-9**, Silica, processes 7790-69-4 11148-13-3 **12033-89-5**, **Silicon nitride**, processes 12070-08-5, Titanium carbide (TiC) 12626-81-2, Lead titanate zirconate 12676-60-7, Lanthanum lead titanium zirconium oxide ((La,Pb)(Ti,Zr)O3) 17861-02-8, Iron nitride (FeN) 24304-00-5, Aluminum nitride (AlN) 25617-97-4, Gallium nitride (GaN) 37303-24-5, Barium strontium titanium oxide (Ba0-1Sr0-1TiO3) 37382-15-3, Aluminum gallium arsenide ((Al,Ga)As) 39361-80-3, Iron zirconium nitride 297772-52-2, Cobalt titanium zirconium oxide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in reative ion-beam **etching** fabrication of magnetic thin film recording head)

IT 75-10-5, **Difluoromethane** **75-46-7**, Fluoroform 75-73-0, Carbon fluoride (**CF4**) 76-16-4, Perfluoroethane **76-19-7** 593-53-3, Methyl fluoride 7782-44-7, Oxygen, processes 10024-97-2, Nitrogen oxide (N2O), processes 10028-15-6, Ozone, processes 10102-44-0, Nitrogen dioxide, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(plasma; in reative ion-beam **etching** fabrication of magnetic thin film recording head)

IT **7631-86-9**, Silica, processes **12033-89-5**, **Silicon nitride**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in reative ion-beam **etching** fabrication of magnetic thin film recording head)

IT **75-46-7**, Fluoroform **76-19-7**
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(plasma; in reative ion-beam **etching** fabrication of magnetic thin film recording head)

L65 ANSWER 15 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2000:85127 HCAPLUS
DOCUMENT NUMBER: 132:130887
TITLE: **Etching** doped **silicon**

dioxide with selectivity to undoped **silicon dioxide** with a high-density plasma **etcher**

INVENTOR(S): Ko, Kei-yu
PATENT ASSIGNEE(S): Micron Technology, Inc., USA
SOURCE: PCT Int. Appl., 49 pp.
CODEN: PIXXD2

DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2000005756	A1	20000203	WO 1998-US15520	19980723
W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
RW: GH, GM, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				
AU 9886642	A1	20000214	AU 1998-86642	19980723
EP 1110238	A1	20010627	EP 1998-938028	19980723
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI				

PRIORITY APPLN. INFO.: WO 1998-US15520 A 19980723

AB Disclosed is a process for removing doped **SiO2** from a structure selectively to undoped **SiO2**. A structure having both doped and undoped **SiO2** regions is exposed to a high-d. plasma **etch** having a fluorinated **etch** chem. Doped **SiO2** is preferably removed thereby at a rate .gtoreq.10 times that of undoped **SiO2**. The **etch** is conducted in a chamber having an upper electrode to which source power is applied and a lower electrode to which bias power is applied, sufficient to generate a power d. on a surface of the structure such that the source power d. is .ltorsim.1000 W per 200-mm-diam. wafer surface. The high-d. plasma **etch** has an ion d. .gtorsim.109 ions/cm3. A variety of structures are formed with the **etch** process, including self-aligned contacts to a **semiconductor** substrate.

IC ICM H01L021-311
CC 76-3 (Electric Phenomena)
ST selective plasma **etching** doped undoped **silicon dioxide**; silica doped undoped selective plasma **etching**
IT **Etching** apparatus
Semiconductor materials
(**etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** with a high-d. plasma **etcher**)
IT Electric contacts
(**etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** with a high-d. plasma **etcher** in formation of)
IT Refractory metal silicides
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in **etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** with a high-d. plasma **etcher**)

IT **Etching**
(plasma; **etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** with a high-d. plasma **etcher**)
IT **7631-86-9, Silicon dioxide**, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(**etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** with a high-d. plasma **etcher**)
IT **12033-89-5, Silicon nitride**, processes
12627-41-7, Tungsten silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in **etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** with a high-d. plasma **etcher**)
IT 75-10-5, **Difluoromethane** **75-46-7**, Fluoroform
75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane
76-19-7, Octafluoropropane 354-33-6, Pentafluoroethane
355-25-9, Perfluorobutane 593-53-3, Fluoromethane
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(plasma **etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** in)
IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; in **etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** with a high-d. plasma **etcher**)
IT **7631-86-9, Silicon dioxide**, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(**etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** with a high-d. plasma **etcher**)
IT **12033-89-5, Silicon nitride**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in **etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** with a high-d. plasma **etcher**)
IT **75-46-7**, Fluoroform **76-19-7, Octafluoropropane**
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(plasma **etching** doped **silicon dioxide** with selectivity to undoped **silicon dioxide** in)
REFERENCE COUNT: 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L65 ANSWER 16 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2000:47009 HCAPLUS
DOCUMENT NUMBER: 132:101609
TITLE: Microwave-activated plasma **etching** of dielectric layers
INVENTOR(S): Merry, Walter Richardson; Brown, William; Herchen, Harald; Welch, Michael D.
PATENT ASSIGNEE(S): Applied Materials, Inc., USA
SOURCE: U.S., 12 pp.
CODEN: USXXAM
DOCUMENT TYPE: Patent

LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6015761	A	20000118	US 1996-672469	19960626

AB A microwave-activated plasma process for **etching** dielec. layers on a substrate with excellent control of the shape and cross-sectional profile of the **etched** features, high **etch** rates, and good **etching** uniformity is described. A process gas comprising (i) fluorocarbon gas (preferably **CF4**), (ii) inorg. fluorinated gas (preferably NF3), and (iii) O is used. The process gas is introduced into a plasma zone remote from a process zone and microwaves are coupled into the plasma zone to form a microwave-activated plasma. The microwave-activated plasma is introduced into the process zone to **etch** the dielec. layer on the substrate with excellent control of the shape of the **etched** features.

IC ICM H01L021-00
NCL 438727000
CC 76-10 (Electric Phenomena)
ST microwave activated plasma **etching** dielec layer; fluorocarbon contg plasma **etching** dielec layer; oxygen contg plasma **etching** dielec layer; nitrogen fluoride contg plasma **etching** dielec layer
IT Hydrocarbons, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fluoro; microwave-activated plasma **etching** of dielec. layers in gas mixts. contg.)
IT Electric insulators
Microwave
(microwave-activated plasma **etching** of dielec. layers)
IT Borophosphosilicate glasses
Phosphosilicate glasses
Silicate glasses
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(microwave-activated plasma **etching** of dielec. layers contg.)
IT **Etching**
(plasma; microwave-activated plasma **etching** of dielec. layers)
IT **7631-86-9**, Silica, processes **12033-89-5**, **Silicon nitride**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(microwave-activated plasma **etching** of dielec. layers contg.)
IT 75-10-5, **Difluoromethane** **75-46-7**, Fluoroform 75-73-0, Carbon fluoride (**CF4**) 76-16-4, Perfluoroethane **76-19-7**, **Perfluoropropane** 115-25-3, Perfluorocyclobutane 354-33-6, Pentafluoroethane 355-25-9, Perfluorobutane 593-53-3, Fluoromethane 2551-62-4, Sulfur fluoride (SF6) 7664-39-3, Hydrogen fluoride, processes 7782-44-7, Oxygen, processes 7783-54-2, Nitrogen fluoride (NF3) **27070-61-7**, **Hexafluoropropane**
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(microwave-activated plasma **etching** of dielec. layers in gas mixts. contg.)
IT **7631-86-9**, Silica, processes **12033-89-5**, **Silicon**

nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(microwave-activated plasma **etching** of dielec. layers contg.)
IT **75-46-7**, Fluoroform **76-19-7**, **Perfluoropropane**
27070-61-7, **Hexafluoropropane**
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(microwave-activated plasma **etching** of dielec. layers in gas mixts. contg.)
REFERENCE COUNT: 22 THERE ARE 22 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L65 ANSWER 17 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 2000:34435 HCAPLUS
DOCUMENT NUMBER: 132:101423
TITLE: Fabrication of **semiconductor** devices in prevention of particle contamination from plasma **etching** chamber
INVENTOR(S): Mihara, Satoru
PATENT ASSIGNEE(S): Fujitsu Ltd., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000012523	A2	20000114	JP 1998-175180	19980622
US 6071828	A	20000606	US 1999-228565	19990112

PRIORITY APPLN. INFO.: JP 1998-175180 19980622

AB Process for plasma **etching** of **semiconductor** substrates in the title fabrication involves depositing a carbonaceous film on the internal wall of plasma **etching** chamber, providing a **semiconductor** substrate in the chamber, and generating plasma contg. a rare gas in the chamber, **impressing** an elec. field so as to attract plasma ions to the substrate surface to be **etched** on its surface. The **etched** material is deposited to the carbonaceous sidewall of the chamber, therefore delamination of contaminant deposits on the wall is prevented.

IC ICM H01L021-3065
CC 76-3 (Electric Phenomena)
ST carbonaceous deposition sidewall **etching** chamber particle delamination **semiconductor** device
IT Delamination
(contaminant particles, prevention of; fabrication of **semiconductor** devices in prevention of particle contamination from plasma **etching** chamber)
IT Carbonaceous materials (technological products)
RL: PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); PRP (Properties); TEM (Technical or engineered material use); PREP (Preparation); PROC (Process); USES (Uses)
(deposition on sidewall; fabrication of **semiconductor** devices in prevention of particle contamination from plasma **etching** chamber)
IT Contamination (electronics)
(**etched** particles; fabrication of **semiconductor** devices in prevention of particle contamination from plasma

etching chamber)
IT **Semiconductor** devices
(fabrication of **semiconductor** devices in prevention of particle contamination from plasma **etching** chamber)
IT Hydrocarbons, uses
RL: RCT (Reactant); TEM (Technical or engineered material use); RACT (Reactant or reagent); USES (Uses)
(fluoro, C3F6, carbonaceous deposition from; fabrication of **semiconductor** devices in prevention of particle contamination from plasma **etching** chamber)
IT Electric field effects
(ion attracting to substrate by; fabrication of **semiconductor** devices in prevention of particle contamination from plasma **etching** chamber)
IT **Semiconductor** materials
(plasma **etching**; fabrication of **semiconductor** devices in prevention of particle contamination from plasma **etching** chamber)
IT **Etching**
(plasma, chamber, contaminant delamination; fabrication of **semiconductor** devices in prevention of particle contamination from plasma **etching** chamber)
IT 74-82-8, Methane, uses 75-10-5, **Difluoromethane** **75-46-7**, Fluoroform 76-16-4 **76-19-7** 115-25-3
RL: RCT (Reactant); TEM (Technical or engineered material use); RACT (Reactant or reagent); USES (Uses)
(carbonaceous deposition from; fabrication of **semiconductor** devices in prevention of particle contamination from plasma **etching** chamber)
IT **75-46-7**, Fluoroform **76-19-7**
RL: RCT (Reactant); TEM (Technical or engineered material use); RACT (Reactant or reagent); USES (Uses)
(carbonaceous deposition from; fabrication of **semiconductor** devices in prevention of particle contamination from plasma **etching** chamber)

L65 ANSWER 18 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1999:238479 HCAPLUS
DOCUMENT NUMBER: 130:290309
TITLE: Anisotropic selective **etching** of nitride of multilayer structure in high-density plasma for high aspect ratio application
INVENTOR(S): Armacost, Michael D.; Wise, Richard Stephan
PATENT ASSIGNEE(S): International Business Machines Corp., USA
SOURCE: Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 11102896	A2	19990413	JP 1998-210482	19980727
JP 3155513	B2	20010409		
US 6051504	A	20000418	US 1997-912216	19970815
EP 908940	A2	19990414	EP 1998-306216	19980805
EP 908940	A3	20000920		

R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO

PRIORITY APPLN. INFO.: US 1997-912216 A 19970815
AB The title method involves exciting an **etchant** gas contg. a fluorocarbon gas such as **CF4**, C2F6 ,or **C3F8**, hydrogen source such as **CH2F2**, CH3F, or H2, and weak oxidant such as CO, CO2, or O2 and applying an elec. power to the structure to control the direction of the high-d. plasma. Specifically, the nitride may comprise Si nitride.
IC ICM H01L021-3065
CC 76-11 (Electric Phenomena)
ST anisotropic selective plasma **etching silicon nitride**
IT Anisotropic **etching**
Plasma **etching**
Selective **etching**
(anisotropic selective **etching** of nitride of multilayer structure in high-d. plasma for high aspect ratio application)
IT Nitrides
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(anisotropic selective **etching** of nitride of multilayer structure in high-d. plasma for high aspect ratio application)
IT Fluoro hydrocarbons
RL: NUU (Other use, unclassified); USES (Uses)
(anisotropic selective **etching** of nitride of multilayer structure in high-d. plasma for high aspect ratio application using)
IT **12033-89-5, Silicon nitride**, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(anisotropic selective **etching** of nitride of multilayer structure in high-d. plasma for high aspect ratio application)
IT 75-10-5, **Difluoromethane** 75-73-0, **Perfluoromethane** 76-16-4, Perfluoroethane **76-19-7, Perfluoropropane** 124-38-9, Carbon dioxide, uses 593-53-3, Monofluoromethane 630-08-0, Carbon monoxide, uses 1333-74-0, Hydrogen, uses 7782-44-7, Oxygen, uses
RL: NUU (Other use, unclassified); USES (Uses)
(anisotropic selective **etching** of nitride of multilayer structure in high-d. plasma for high aspect ratio application using)
IT **12033-89-5, Silicon nitride**, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(anisotropic selective **etching** of nitride of multilayer structure in high-d. plasma for high aspect ratio application)
IT **76-19-7, Perfluoropropane**
RL: NUU (Other use, unclassified); USES (Uses)
(anisotropic selective **etching** of nitride of multilayer structure in high-d. plasma for high aspect ratio application using)

L65 ANSWER 21 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1998:728676 HCAPLUS
DOCUMENT NUMBER: 129:349831
TITLE: Undoped **silicon dioxide** as an **etch** stop for selective **etching** of doped **silicon dioxide**
INVENTOR(S): Ko, Kei-yu
PATENT ASSIGNEE(S): Micron Technology, Inc., USA
SOURCE: PCT Int. Appl., 32 pp.
CODEN: PIXXD2
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 9849719	A1	19981105	WO 1998-US2826	19980216
W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
RW: GH, GM, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG				
AU 9861646	A1	19981124	AU 1998-61646	19980216
EP 1004139	A1	20000531	EP 1998-906417	19980216
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI				
JP 2001522531	T2	20011113	JP 1998-546947	19980216
PRIORITY APPLN. INFO.:			US 1997-846671 A	19970430
			WO 1998-US2826 W	19980216

AB The invention relates to a process for selectively plasma **etching** a structure on a **semiconductor** substrate to form a designated topog. structure using an undoped **SiO2** layer as an **etch** stop. In 1 embodiment, a substantially undoped **SiO2** layer is formed on a layer of **semiconductor** material. A doped **SiO2** layer is then formed on the undoped **SiO2** layer. The doped **SiO2** layer is **etched** to create the topog. structure. The **etch** has a material removal rate that is .gtoreq.10 times higher for doped **SiO2** than for undoped **SiO2** or the **semiconductor** material.

IC ICM H01L021-302

CC 76-3 (Electric Phenomena)

ST undoped silica **etch** stop; selective plasma **etching** doped silica

IT Plasma **etching**
Reactive ion **etching**
(of doped silica using undoped silica as **etch** stop)

IT Selective **etching**
(selective **etching** of doped silica using undoped silica as **etch** stop)

IT Refractory metal silicides
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(selective **etching** of doped silica using undoped silica as **etch** stop on substrates contg.)

IT **Semiconductor** materials
(selective **etching** of doped silica using undoped silica as **etch** stop on substrates from)

IT Borophosphosilicate glasses
Borosilicate glasses
Phosphosilicate glasses
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(undoped **silicon dioxide** as **etch** stop for selective plasma **etching** of)

IT 7440-21-3, Silicon, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(polycryst.; selective **etching** of doped silica using undoped silica as **etch** stop on substrates contg.)

IT 12627-41-7, Tungsten silicide
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(selective **etching** of doped silica using undoped silica as **etch** stop on substrates contg.)

IT 75-10-5, **Difluoromethane 75-46-7**,

Trifluoromethane 75-73-0, Carbon tetrafluoride 76-16-4, Perfluoroethane **76-19-7**, **Perfluoropropane** 354-33-6, Pentafluoroethane 355-25-9, Perfluorobutane 593-53-3, Fluoromethane
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(selective plasma **etching** of doped silica in)

IT **7631-86-9**, Silica, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(selective plasma **etching** of doped silica using undoped silica as **etch** stop)

IT **75-46-7**, **Trifluoromethane 76-19-7**, **Perfluoropropane**
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(selective plasma **etching** of doped silica in)

IT **7631-86-9**, Silica, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(selective plasma **etching** of doped silica using undoped silica as **etch** stop)

L65 ANSWER 24 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1997:666928 HCAPLUS
DOCUMENT NUMBER: 127:313859
TITLE: Anisotropic dry **etching** of borophosphosilicate glasses in high selectivity
INVENTOR(S): Harashima, Keiichi
PATENT ASSIGNEE(S): NEC Corp., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09266198	A2	19971007	JP 1996-74103	19960328
JP 2836569	B2	19981214		

AB Title process, for selective **etching** of BPSG or PSG films vs. silica films, uses C- and F-contg. compds. as **etching** gases and **CH2F2** as additive gases.

IC ICM H01L021-3065
ICS C23F004-00

CC 76-3 (Electric Phenomena)

ST borophosphosilicate glass anisotropic **etching** selectivity; fluoromethane additive gas anisotropic BPSG **etching**

IT Electric contacts
(anisotropic dry **etching** of borophosphosilicate glasses for elec.-contact formation)

IT Borophosphosilicate glasses
Phosphosilicate glasses
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(anisotropic dry **etching** of borophosphosilicate glasses in high selectivity)

IT Dry **etching**
(anisotropic; anisotropic dry **etching** of borophosphosilicate glasses in high selectivity)

IT Anisotropic **etching**
(dry; anisotropic dry **etching** of borophosphosilicate glasses in high selectivity)

IT 75-10-5, **Difluoromethane**

RL: MOA (Modifier or additive use); USES (Uses)
(additive gas; anisotropic dry **etching** of borophosphosilicate glasses in high selectivity)

IT **75-46-7, Trifluoromethane** 75-73-0, **Perfluoromethane** 76-16-4, Perfluoroethane **76-19-7, Perfluoropropane**
RL: NUU (Other use, unclassified); USES (Uses)
(**etching** gas; anisotropic dry **etching** of borophosphosilicate glasses in high selectivity)

IT **7631-86-9**, Silica, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(**etching**-stopper film; anisotropic dry **etching** of borophosphosilicate glasses in high selectivity)

IT **75-46-7, Trifluoromethane 76-19-7, Perfluoropropane**
RL: NUU (Other use, unclassified); USES (Uses)
(**etching** gas; anisotropic dry **etching** of borophosphosilicate glasses in high selectivity)

IT **7631-86-9**, Silica, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(**etching**-stopper film; anisotropic dry **etching** of borophosphosilicate glasses in high selectivity)

L65 ANSWER 26 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1997:464967 HCAPLUS
DOCUMENT NUMBER: 127:89284
TITLE: Plasma **etching** of oxide with high selectivity to nitride suitable for use on surfaces of uneven topography
INVENTOR(S): Yang, Chan-Lon; Chang, Mei; Arleo, Paul; Li, Haojiang; Levinstein, Hyman
PATENT ASSIGNEE(S): Applied Materials, Inc., USA
SOURCE: Eur. Pat. Appl., 9 pp.
CODEN: EPXXDW
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 28
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
EP 777267	A1	19970604	EP 1996-117494	19961031
R: AT, BE, CH, DE, ES, FR, GB, GR, IE, IT, LI, NL, SE				
JP 09172005	A2	19970630	JP 1996-309066	19961120
US 5849136	A	19981215	US 1996-754833	19961122
PRIORITY APPLN. INFO.:			US 1995-565184 A	19951128
			US 1991-774127 A3	19911011
			US 1993-984234 B1	19930201
			US 1995-433002 B1	19950503

AB A plasma **etching** process is described for the **etching** of oxide with a high selectivity to nitride, including nitride formed on uneven surfaces of a substrate, e.g., on sidewalls of steps on an **integrated circuit** structure. The addn. of a H-contg. gas to C4F8 or C2F6 **etch** gases and a scavenger for F results in a high selectivity to nitride which is preserved regardless of the topog. of the nitride portions of the substrate surface.

IC ICM H01L021-311
CC 76-3 (Electric Phenomena)

ST plasma **etching** oxide nitride selective; uneven topog plasma **etching** oxide; **integrated circuit** plasma **etching** oxide

IT Sputter **etching**
(plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

IT Nitrides
RL: MSC (Miscellaneous)
(plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

IT Oxides (inorganic), processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

IT **Integrated circuits**
(plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog. in)

IT 74-86-2, Acetylene, processes 75-10-5, **Difluoromethane** 593-53-3, Monofluoromethane
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(**etching** gas contg.; in plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

IT 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7, Octafluoropropane** 11070-66-9, Octafluorobutene
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(**etching** gas; in plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

IT 7440-21-3, Silicon, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(fluorine scavenger and substrate; in plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

IT 7440-44-0, Carbon, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(fluorine scavenger; in plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

IT **12033-89-5, Silicon nitride (Si3N4)**, miscellaneous
RL: MSC (Miscellaneous)
(plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

IT **7631-86-9**, Silica, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

IT **76-19-7, Octafluoropropane**
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(**etching** gas; in plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

IT **12033-89-5, Silicon nitride (Si3N4)**, miscellaneous
RL: MSC (Miscellaneous)
(plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

IT **7631-86-9**, Silica, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(plasma **etching** of oxide with high selectivity to nitride on surfaces of uneven topog.)

L65 ANSWER 27 OF 39 HCAPLUS COPYRIGHT 2002 ACS

ACCESSION NUMBER: 1997:449036 HCAPLUS
DOCUMENT NUMBER: 127:74421
TITLE: Manufacture of **semiconductor** device by dry-**etching**
INVENTOR(S): Imai, Shinichi; Jiwari, Nobuhiko
PATENT ASSIGNEE(S): Matsushita Electronics Corp., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09162162	A2	19970620	JP 1995-318793	19951207

AB The device is manufd. by (1) contact-hole **etching** of an oxide film on a Si substrate and (2) applying high frequency power to the substrate by feeding an O gas at .gtoreq.10 m Torr or an O-free **etching** gas contg. C, F, or H at .gtoreq.50 m Torr into its **etching** app. The device shows low contact resistivity.
IC ICM H01L021-3065
CC 76-3 (Electric Phenomena)
ST **semiconductor** device dry **etching** oxide film
IT Dry **etching**
Semiconductor device fabrication
(dry **etching** of oxide film in manuf. of **semiconductor** device with low contact resistivity)
IT **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(dry **etching** of oxide film in manuf. of **semiconductor** device with low contact resistivity)
IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(dry **etching** of oxide film in manuf. of **semiconductor** device with low contact resistivity)
IT 75-10-5, **Difluoro methane** **75-46-7**, **Trifluoro methane** 76-16-4 7782-44-7, Oxygen, uses
RL: NUU (Other use, unclassified); USES (Uses)
(dry **etching** of oxide film in manuf. of **semiconductor** device with low contact resistivity)
IT **76-19-7**, **Octafluoropropane** 11070-66-9, Perfluorobutene
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(dry **etching** of oxide film in manuf. of **semiconductor** device with low contact resistivity)
IT **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(dry **etching** of oxide film in manuf. of **semiconductor** device with low contact resistivity)
IT **75-46-7**, **Trifluoro methane**
RL: NUU (Other use, unclassified); USES (Uses)
(dry **etching** of oxide film in manuf. of **semiconductor** device with low contact resistivity)
IT **76-19-7**, **Octafluoropropane**
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(dry **etching** of oxide film in manuf. of **semiconductor** device with low contact resistivity)

L65 ANSWER 28 OF 39 HCAPLUS COPYRIGHT 2002 ACS

ACCESSION NUMBER: 1995:986937 HCAPLUS
DOCUMENT NUMBER: 124:103886
TITLE: Manufacture of **semiconductor** devices
INVENTOR(S): Matsunaga, Daisuke; Hashimi, Kazuo; Komuro, Genichi
PATENT ASSIGNEE(S): Fujitsu Ltd, Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 07263415	A2	19951013	JP 1994-48878	19940318
US 5830807	A	19981103	US 1997-866046	19970530
PRIORITY APPLN. INFO.:			JP 1994-48878	19940318
			US 1995-404523	19950315

AB The devices are manufd. by formation of **etching** masks on alternate laminates of Si and **SiO2**, followed by **etching** of Si or **SiO2** with mixts. of .gtoreq.1 gases selected from 2 of the groups of (a) NF3, **CF4**, and SF6, (b) CO, **CHF3**, **CH2F2**, C2F6, **C3F8**, and C4F8, and (c) Cl2, HBr, and Br2, and **etching** of the other layers with mixts. of the same gases having different ratio. The process is esp. useful in fabrication of devices having multilayered capacitors, e.g. DRAMs.

IC ICM H01L021-3065
ICS C23F004-00; H01L021-266; H01L021-316; H01L021-8242; H01L027-108
CC 76-3 (Electric Phenomena)
ST silicon silica alternate laminate **etching**; DRAM silicon silica dry **etching**
IT **Semiconductor** devices
(manuf. of **semiconductor** devices by dry **etching** of silicon/silica alternate laminates)
IT Electric capacitors
(multilayered; manuf. of **semiconductor** devices by dry **etching** of silicon/silica alternate laminates)
IT **Etching**
(dry, manuf. of **semiconductor** devices by dry **etching** of silicon/silica alternate laminates)
IT 75-10-5, **Difluoromethane** **75-46-7**, **Trifluoromethane** 75-73-0, Carbon tetrafluoride 76-16-4, Perfluoroethane **76-19-7**, **Perfluoropropane** 630-08-0, Carbon monoxide, uses 2551-62-4, Sulfur hexafluoride 7726-95-6, Bromine, uses 7782-50-5, Chlorine, uses 7783-54-2, Nitrogen trifluoride 10035-10-6, Hydrobromic acid, uses 11070-66-9, Perfluorobutene
RL: TEM (Technical or engineered material use); USES (Uses)
(**etchant**; manuf. of **semiconductor** devices by dry **etching** of silicon/silica alternate laminates)
IT 7440-21-3, Silicon, processes **7631-86-9**, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(manuf. of **semiconductor** devices by dry **etching** of silicon/silica alternate laminates)
IT **75-46-7**, **Trifluoromethane** **76-19-7**, **Perfluoropropane**
RL: TEM (Technical or engineered material use); USES (Uses)
(**etchant**; manuf. of **semiconductor** devices by dry **etching** of silicon/silica alternate laminates)

IT **7631-86-9**, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(manuf. of **semiconductor** devices by dry **etching** of silicon/silica alternate laminates)

L65 ANSWER 29 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1995:986936 HCAPLUS
DOCUMENT NUMBER: 124:133083
TITLE: Dry **etching** of **silicon oxide** film for manufacture of **semiconductor** device
INVENTOR(S): Ito, Satoru; Kanai, Saburo; Hamazaki, Ryoji; Okamura, Koichi; Sato, Yoshe; Tokunaga, Takafumi; Usui, Taketo; Nawata, Makoto
PATENT ASSIGNEE(S): Hitachi Ltd, Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 07263409	A2	19951013	JP 1994-46819	19940317
JP 3223692	B2	20011029		

AB A Si oxide film, obtained by generating plasma by microwave and magnetic field and applying high-frequency elec. power to an electrode on a **semiconductor** substrate, is dry **etched** with CxFy and O. A Si oxide film is **etched** with high selectivity and stability.
IC ICM H01L021-3065
ICS C23F004-00
CC 76-3 (Electric Phenomena)
ST dry **etching silicon oxide semiconductor**; fluorocarbon oxygen **etching silicon oxide**
IT **Etching**
Semiconductor devices
(dry **etching** of **silicon oxide** with fluorocarbon and oxygen for manuf. of **semiconductor** device)
IT 7782-44-7, Oxygen, processes
RL: MOA (Modifier or additive use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(dry **etching** of **silicon oxide** with fluorocarbon and oxygen for manuf. of **semiconductor** device)
IT 75-10-5, **Difluoromethane 75-46-7**, **Trifluoromethane** 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane 26447-60-9 27070-61-7** 51000-94-3
RL: NUU (Other use, unclassified); USES (Uses)
(dry **etching** of **silicon oxide** with fluorocarbon and oxygen for manuf. of **semiconductor** device)
IT **11126-22-0, Silicon oxide**
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(dry **etching** of **silicon oxide** with fluorocarbon and oxygen for manuf. of **semiconductor** device)
IT **75-46-7, Trifluoromethane 76-19-7, Octafluoropropane 26447-60-9 27070-61-7**

RL: NUU (Other use, unclassified); USES (Uses)
(dry **etching** of **silicon oxide** with
fluorocarbon and oxygen for manuf. of **semiconductor** device)

IT **11126-22-0, Silicon oxide**
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(dry **etching** of **silicon oxide** with
fluorocarbon and oxygen for manuf. of **semiconductor** device)

L65 ANSWER 30 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1995:689991 HCAPLUS
DOCUMENT NUMBER: 123:72391
TITLE: Plasma **etching** of oxide in the presence of nitride
INVENTOR(S): Yang, Chan Lon; Marks, Jeffrey; Bright, Nicolas; Collins, Kenneth S.; Groechel, David; Keswick, Peter
PATENT ASSIGNEE(S): Applied Materials, Inc., USA
SOURCE: Eur. Pat. Appl., 9 pp.
CODEN: EPXXDW
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 28
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
EP 651434	A2	19950503	EP 1994-117087	19941028
EP 651434	A3	19960731		
R: BE, CH, DE, ES, FR, GB, IE, IT, LI, NL, SE				
JP 07161702	A2	19950623	JP 1994-245137	19941011
US 5849136	A	19981215	US 1996-754833	19961122

PRIORITY APPLN. INFO.:
US 1993-145894 A 19931029
US 1991-774127 A3 19911011
US 1993-984234 B1 19930201
US 1995-433002 B1 19950503

AB A plasma **etch** process is described for the **etching** of oxide with a high selectivity to nitride, including nitride formed on uneven surfaces of a substrate, e.g., on sidewalls of steps on an **integrated circuit** structure. The addn. of .gtoreq.1 H-contg. gases, preferably .gtoreq.1 hydrofluorocarbon gases, to .gtoreq.1 F-substituted hydrocarbon **etch** gases and a scavenger for F, in a plasma **etch** process for **etching** oxide in preference to nitride, results in a high selectivity to nitride which is preserved regardless of the topog. of the nitride portions of the substrate surface. In a preferred embodiment, .gtoreq.1 O-bearing gases are also added to reduce the overall rate of polymer deposition on the chamber surfaces and on the surfaces to be **etched,** which can otherwise reduce the **etch** rate and cause excessive polymer deposition on the chamber surfaces. The F scavenger is preferably an elec. grounded Si electrode assocd. with the plasma.

IC ICM H01L021-311
CC 76-3 (Electric Phenomena)
ST plasma **etching** oxide; nitride selective plasma **etching** oxide
IT Nitrides
Oxides, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(plasma **etching** of oxide in presence of nitride)
IT Perfluorocarbons
RL: PEP (Physical, engineering or chemical process); PROC (Process)

(plasma **etching** of oxide in presence of nitride in gas mixts. contg.)
IT Sputtering
(**etching**, plasma **etching** of oxide in presence of nitride)
IT Hydrocarbons, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(fluoro, plasma **etching** of oxide in presence of nitride in gas mixts. contg.)
IT **Electric circuits**
(**integrated**, plasma **etching** of oxide in presence of nitride in manuf. of)
IT **Etching**
(sputter, plasma **etching** of oxide in presence of nitride)
IT 7440-21-3, Silicon, uses 7440-44-0, Carbon, uses
RL: NUU (Other use, unclassified); USES (Uses)
(fluorine scavenger in plasma **etching** of oxide in presence of nitride)
IT **7631-86-9**, Silica, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(plasma **etching** of oxide in presence of nitride)
IT 75-10-5, **Difluoromethane 75-46-7**, **Trifluoromethane** 76-16-4, Perfluoroethane **76-19-7**, **Perfluoropropane** 124-38-9, Carbon dioxide, processes 593-53-3, Monofluoromethane 630-08-0, Carbon monoxide, processes 7782-44-7, Oxygen, processes 10028-15-6, Ozone, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(plasma **etching** of oxide in presence of nitride in gas mixts. contg.)
IT **12033-89-5**, **Silicon nitride (Si3N4)**, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(plasma **etching** of silica in presence of)
IT **7631-86-9**, Silica, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(plasma **etching** of oxide in presence of nitride)
IT **75-46-7**, **Trifluoromethane 76-19-7**, **Perfluoropropane**
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(plasma **etching** of oxide in presence of nitride in gas mixts. contg.)
IT **12033-89-5**, **Silicon nitride (Si3N4)**, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(plasma **etching** of silica in presence of)

L65 ANSWER 31 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1995:630517 HCAPLUS
DOCUMENT NUMBER: 123:45934
TITLE: **Etching** of electric insulator films for **semiconductor** devices
INVENTOR(S): Nabeshima, Tamotsu; Tamaoki, Norihiko
PATENT ASSIGNEE(S): Matsushita Electric Ind Co Ltd, Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 07099188	A2	19950411	JP 1994-167901	19940720

PRIORITY APPLN. INFO.: JP 1993-191105 19930802

AB The method involves the following steps; forming a metal film on a **semiconductor** substrate, an insulating film on the metal film, and a patterned mask on the insulating film, **etching** with an O-free gas contg. N2 to open a hole in the insulating film, and removing the mask. This method is useful for formation of contact holes in manuf. of **semiconductor** devices. Formation of metal oxides was prevented.

IC ICM H01L021-3065
ICS H01L021-28; H01L021-3213

CC 76-3 (Electric Phenomena)

ST **etching** nitrogen elec insulator **semiconductor**

IT Electric insulators and Dielectrics
Etching
Semiconductor devices
(**etching** of elec. insulator with nitrogen-contg. gas for manuf. of **semiconductor** device)

IT 74-82-8, Methane, processes 75-10-5, **Difluoromethane** **75-46-7, Trifluoromethane** 75-73-0, **Tetrafluoromethane** 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane** 593-53-3, Monofluoromethane 2551-62-4, Hexafluorosulfur 11070-66-9, Octafluorobutene
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant; etching** of elec. insulator with nitrogen-contg. gas for manuf. of **semiconductor** device)

IT 7727-37-9, Nitrogen, processes
RL: MOA (Modifier or additive use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etching** of elec. insulator with nitrogen-contg. gas for manuf. of **semiconductor** device)

IT 1333-74-0, Hydrogen, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etching** of elec. insulator with nitrogen-contg. gas for manuf. of **semiconductor** device)

IT **75-46-7, Trifluoromethane 76-19-7, Octafluoropropane**
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**etchant; etching** of elec. insulator with nitrogen-contg. gas for manuf. of **semiconductor** device)

L65 ANSWER 32 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1995:499797 HCAPLUS
DOCUMENT NUMBER: 122:304575
TITLE: **Semiconductor** devices and their manufacture
INVENTOR(S): Kokubu, Takashi
PATENT ASSIGNEE(S): Seiko Epson Corp, Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

JP 07029988 A2 19950131 JP 1993-168187 19930707

AB The devices have holes, formed on source-drain region, with different area sizes depending on max. depth of source-drain impurity concn. Th devices are manufd. by processes including gas plasma **etching** of insulating layer with CxFy and CxHyFz. Overetching of Si substrates are controlled.

IC ICM H01L021-8238
ICS H01L027-092; H01L021-3065; H01L029-78; H01L021-336

CC 76-3 (Electric Phenomena)

ST **semiconductor** device hole formation; gas plasma **etching** hole **semiconductor**; carbon fluoride **etchant** **semiconductor** device; hydrocarbon fluoride **etchant** **semiconductor** device

IT Electric insulators and Dielectrics
(formation of holes in insulators by gas plasma **etching** with fluorocarbons and fluorohydrocarbons in **semiconductor** device manuf.)

IT Perfluorocarbons
RL: TEM (Technical or engineered material use); USES (Uses)
(formation of holes in insulators by gas plasma **etching** with fluorocarbons and fluorohydrocarbons in **semiconductor** device manuf.)

IT **Semiconductor** devices
(holes; formation of holes in insulators by gas plasma **etching** with fluorocarbons and fluorohydrocarbons in **semiconductor** device manuf.)

IT **Etching**
(plasma gas; formation of holes in insulators by gas plasma **etching** with fluorocarbons and fluorohydrocarbons in **semiconductor** device manuf.)

IT Hydrocarbons, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(fluoro, formation of holes in insulators by gas plasma **etching** with fluorocarbons and fluorohydrocarbons in **semiconductor** device manuf.)

IT 75-10-5, **Difluoromethane** **75-46-7**, **Trifluoromethane** 75-73-0, **Tetrafluoromethane** 76-16-4, Perfluoroethane **76-19-7**, **Perfluoropropane**
RL: TEM (Technical or engineered material use); USES (Uses)
(formation of holes in insulators by gas plasma **etching** with fluorocarbons and fluorohydrocarbons in **semiconductor** device manuf.)

IT **75-46-7**, **Trifluoromethane** **76-19-7**, **Perfluoropropane**
RL: TEM (Technical or engineered material use); USES (Uses)
(formation of holes in insulators by gas plasma **etching** with fluorocarbons and fluorohydrocarbons in **semiconductor** device manuf.)

L65 ANSWER 34 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1994:287533 HCAPLUS
DOCUMENT NUMBER: 120:287533
TITLE: Dry **etching**
INVENTOR(S): Yanagida, Toshiharu
PATENT ASSIGNEE(S): Sony Corp, Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05326460	A2	19931210	JP 1993-17617	19930204
US 5445712	A	19950829	US 1993-29534	19930311
PRIORITY APPLN. INFO.:			JP 1992-67111	19920325
			JP 1992-67112	19920325

AB Si compd. layers are **etched** with inorg. halide gases (A) contg. .gtoreq.1 functional groups selected from CO, SO, SO2, nitrosyl, or nitryl. Optionally, the **etchants** contain fluorocarbon compds. (B). Two-step **etching** process comprising just **etching** with A and B and over **etching** A and B of higher A/B ratio than the just **etching** process is also claimed. Dry **etching** is carried out at high selectivity without contamination.

IC ICM H01L021-302
ICS H01L021-28

CC 76-3 (Electric Phenomena)

ST dry **etching** silicon compd layer; halide **etchant** dry process; fluorocarbon **etchant** dry process

IT **Etching**
(dry, of silicon compds., halides for)

IT Hydrocarbons, uses
RL: USES (Uses)
(fluoro, **etchant**, dry, with halides, for silicon compds.)

IT 353-50-4, Carbonyl fluoride 359-40-0, Oxalyl fluoride 2699-79-8, Sulfuryl fluoride 5714-22-7, Sulfur fluoride (s2f10) 7783-42-8, Thionyl fluoride 7783-60-0, Sulfur fluoride (SF4) 7789-25-5, Nitrosyl fluoride 10022-50-1, Nitryl fluoride 13709-35-8, Sulfur fluoride (s2f2) 13814-25-0, Sulfur fluoride (SF2)
RL: USES (Uses)
(**etchant**, dry, for silicon compds.)

IT 75-10-5, **Difluoromethane 75-46-7**, **Trifluoromethane** 75-73-0, **Tetrafluoromethane 76-19-7**, **Perfluoropropane** 115-25-3, Octafluorocyclobutane 593-53-3, Fluoromethane
RL: USES (Uses)
(**etchant**, dry, with halides, for silicon compds.)

IT **7631-86-9**, Silica, reactions
RL: RCT (Reactant)
(**etching** of, dry, halides for)

IT **75-46-7**, **Trifluoromethane 76-19-7**, **Perfluoropropane**
RL: USES (Uses)
(**etchant**, dry, with halides, for silicon compds.)

IT **7631-86-9**, Silica, reactions
RL: RCT (Reactant)
(**etching** of, dry, halides for)

L65 ANSWER 35 OF 39 HCAPLUS COPYRIGHT 2002 ACS
ACCESSION NUMBER: 1993:507280 HCAPLUS
DOCUMENT NUMBER: 119:107280
TITLE: Method for selectively **etching** a III-V **semiconductor**, in the production of a field-effect transistor
INVENTOR(S): Mizunuma, Yasuyuki
PATENT ASSIGNEE(S): Sony Corp., Japan
SOURCE: Eur. Pat. Appl., 10 pp.
CODEN: EPXXDW
DOCUMENT TYPE: Patent

LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
EP 533203	A2	19930324	EP 1992-116042	19920918
R: DE, FR, GB				
JP 05082560	A2	19930402	JP 1991-268536	19910920
US 5389574	A	19950214	US 1993-136597	19931014

PRIORITY APPLN. INFO.: JP 1991-268536 19910920
US 1992-946607 19920918

AB A selective **etching** uses a mixed gas comprising a gas contg. C and F as constituents and a gas contg. Si and Cl as constituents. A III-V compd. free of Al is adjacent to an Al-contg. III-V compd. The gas contg. C and F is at least a fluorocarbon-based gas selected from **CF4**, C2F6, **C3F8**, **CHF3**, **CH2F2**, and CBrF3. The gas contg. Si and Cl is .gtoreq.1 silane-based gas selected from SiCl4, SiH2Cl2 and SiHCl3. In particular, **CF4** and SiCl4 are used. A GaAs-based compd. **semiconductor** on (Al,Ga)As-based compd. **semiconductor** is **etched**. High selectivity is achieved with low power and less damage.

IC ICM H01L021-306
ICS H01L021-338; H01L021-28

CC 76-3 (Electric Phenomena)

ST **etching** Group III V **semiconductor**; transistor
etching pnictide

IT Transistors
(**etching** of gallium arsenide-aluminum gallium arsenide structures for)

IT **Etching**
(selective, of gallium arsenide-aluminum gallium arsenide structures for transistors)

IT 75-10-5, **Difluoromethane 75-46-7**, **Trifluoromethane** 75-63-8, Bromotrifluoromethane 75-73-0, Carbon tetrafluoride 76-16-4, Hexafluoroethane **76-19-7**, **Octafluoropropane** 4109-96-0, Dichlorosilane 10025-78-2, Trichlorosilane 10026-04-7, Tetrachlorosilane
RL: TEM (Technical or engineered material use); USES (Uses)
(**etchant**, for gallium arsenide-aluminum gallium arsenide structures for transistors)

IT 1303-00-0, Gallium arsenide, reactions
RL: TEM (Technical or engineered material use); USES (Uses)
(**etching** of structures from aluminum gallium arsenide and, for transistors)

IT 37382-15-3, Aluminum gallium arsenide ((Al,Ga)As)
RL: TEM (Technical or engineered material use); USES (Uses)
(**etching** of structures from gallium arsenide and, for transistors)

IT **75-46-7**, **Trifluoromethane 76-19-7**, **Octafluoropropane**
RL: TEM (Technical or engineered material use); USES (Uses)
(**etchant**, for gallium arsenide-aluminum gallium arsenide structures for transistors)